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DIGITAL DATA ACQUISITION SYSTEM FOR USE IN AIRCRAFT ENGINE COND--ETC(U)
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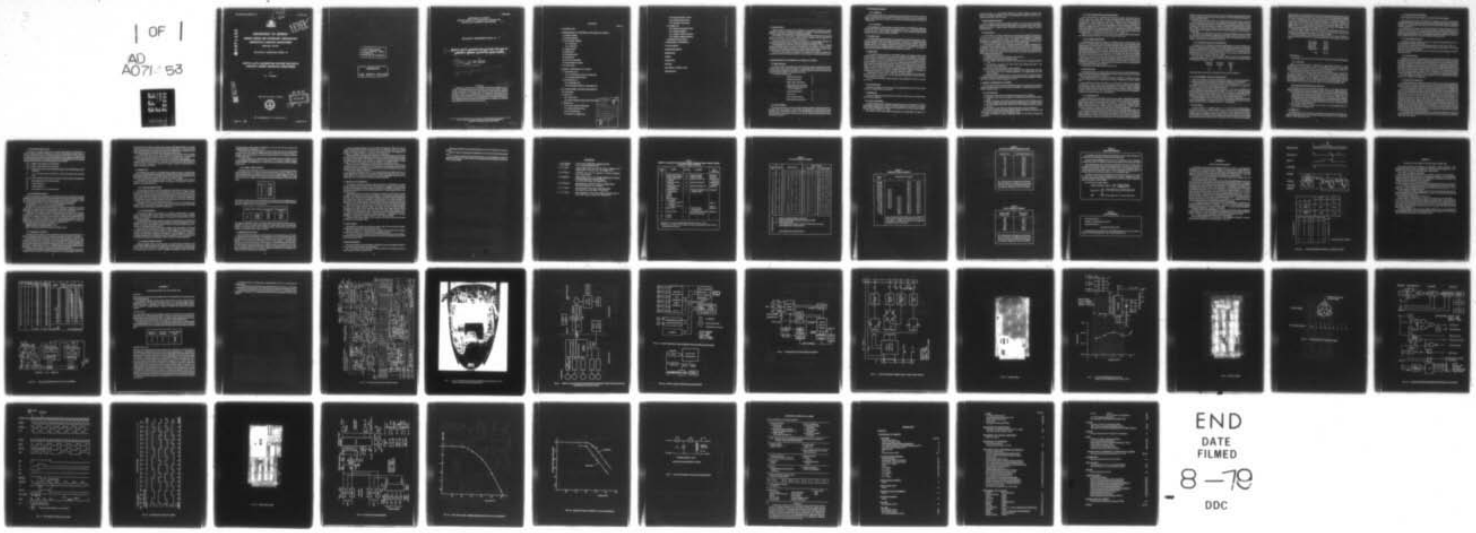

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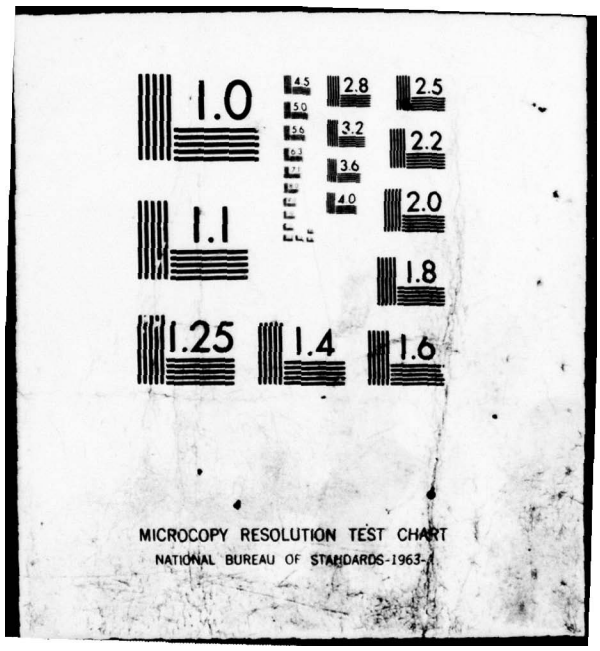
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MECHANICAL ENGINEERING REPORT 151

DIGITAL DATA ACQUISITION SYSTEM FOR USE IN AIRCRAFT ENGINE CONDITION MONITORING

by

M. T. ADAMS

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MECHANICAL ENGINEERING REPORT 151

(6) DIGITAL DATA ACQUISITION SYSTEM FOR USE IN AIRCRAFT ENGINE CONDITION MONITORING

by

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SUMMARY

A digital data acquisition system is described which has been developed as part of a project to investigate assessment of aircraft engine condition from in-flight recording of a number of parameters. The recording system is based on a small inexpensive audio tape recorder, and accepts up to 12 analogue inputs and 4 digital inputs. Recording of data in digital form is made on a standard cassette using a novel frequency coding technique. Other novel aspects of the system are the successful application of a computer-like architecture to an essentially simple system and the ease with which data can be displayed for calibration and pre-flight checks with simple hand held test gear.

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CONTENTS

	Page No.
1. INTRODUCTION	1
2. REQUIREMENTS OF RECORDER AND CHOICE OF SYSTEM	1
2.1 Engine Parameters	1
2.2 Aircraft Installation	1
2.3 Environmental Conditions	2
2.3.1 Temperature	2
2.3.2 Acceleration	2
2.4 Analogue Inputs	2
2.5 Digital Inputs	2
2.6 Recording Duration	2
2.7 Sampling Rate	2
2.8 Accuracy and Resolution	2
2.9 Data Handling and Analysis	3
2.10 System Choice	3
3. GENERAL DESCRIPTION OF SYSTEM	
3.1 Aircraft Sub-system	3
3.1.1 16 CAD Recorder as part of the Sub-system	4
3.1.2 The Digital Signal Monitor	4
3.2 Ground Sub-system	4
3.2.1 Transcription Unit	4
3.2.2 Output Signal Monitor for Transcription Unit	5
4. 16 CAD RECORDER—DETAILED DESCRIPTION	5
4.1 Power Supply	5
4.2 Clock Card	6
4.2.1 Crystal Clock	6
4.2.2 Other Functions Performed on the Clock Card	6
4.3 Digital Card	6
4.3.1 Ternary Frequency Shift Keying	7
4.3.2 Format of Record on Tape	7
4.3.3 Data Sample Rate	7
4.3.4 Data Flow on Digital Card	7

4.3.5 Read Only Memory Control 8
4.3.6 Channel Sampie Sequence 8
4.3.7 Generation of Wave-forms 8
4.4 Analogue Card 9
4.4.1 Channel Interrogation Circuitry 9
4·4.2 Analogue Multiplexer 9
4.4.3 Analogue to Digital Conversion 9
4.4.4 Analogue Calibration Reference 10
4.5 Digital Bus and Its Protocol 10
5. OPERATIONAL EXPERIENCE 11
6. CONCLUSIONS 11
ACKNOWLEDGMENTS
REFERENCES
TABLES
APPENDICES
FIGURES
DOCUMENT CONTROL DATA
DISTRIBUTION

1. INTRODUCTION

Engine Condition Monitoring may be defined as the systematic observation of engine behaviour with a view to assessing the capability of the engine to continue functioning satisfactorily as regards both performance and mechanical condition.

The eventual aim of monitoring is to enable assessment of engine condition so that a rational decision can be made on the need for overhaul, with the expectation that this approach will prove to be more economical than scheduled maintenance.

Monitoring comprises all procedures and techniques for observing engine condition and behaviour ranging from inspection to flight data recording and analysis (FDRA).

Following exploratory work done by these laboratories with FDRA in 1973 on a Mirage aircraft instrumented mainly for structural investigations, it was agreed in 1974 by the Royal Australian Air Force that a Macchi trainer be made available for an Engine Condition Monitoring programme. The Macchi trainers are powered by Viper turbojet engines.

The data recording system here described was developed for an initial investigation into a particular method by which engine condition may be monitored by performance trend analysis.

2. REQUIREMENTS OF RECORDER AND CHOICE OF SYSTEM

2.1 Engine Parameters

For the first trials, it was decided that only the minimum number of parameters would be recorded which would permit trend analysis of engine performance. Mechanical aspects such as oil temperature and pressure, and vibration would be excluded. However, provision has been made for further parameters to be added at a later date.

The selected parameters were:

ambient static pressure	P_s
ambient pitot pressure	P_t
engine intake total pressure	P_1
engine intake total temperature (assumed equivalent to external total air temperature)	T_1
engine rotational speed	N
fuel flow rate	F
exhaust gas total pressure	P_4
exhaust gas total temperature	T_4

2.2 Aircraft Installation

The Macchi aircraft was to be used in regular training operations and the system was not to interfere with these operations. For this reason, the equipment was mounted in the forward instrument bay of the aircraft: see Figure 1. This location placed a severe restriction on the size and weight of the equipment which could be used, the available uncommitted space being of the order of 20 litres.

2.3 Environmental Conditions

2.3.1 Temperature

The forward instrument bay is unpressurised and isolated from the external environment only by the aluminium skin of the aircraft. The temperature extremes in the bay were measured during a week's flying using a minimum and maximum recording thermometer and found to be −20°C to 70°C.

2.3.2 Acceleration

The equipment as a whole, of which the cassette recorder was considered the critical component, must operate when subjected to accelerations of +9 g to −3 g. Previous experience in a Mirage[1] with a similar recorder demonstrated that this was feasible, provided that the optimum orientation of the recorder was selected.

2.4 Analogue Inputs

Six of the parameters listed in Section 2.1 are measured as analogue voltage signals. Table 1 lists the transducers which provide these signals and a reference to the signal conditioning associated with each. To allow for additional parameters it was decided to provide 12 analogue channels. Because of the number of channels, the disposition of the transducers around the aircraft and the lack of knowledge regarding the cables within the aircraft, it was decided to provide differential inputs. The signal level to be accepted was ±5 Volt.

2.5 Digital Inputs

It was decided to make provision for direct digital inputs to the proposed recorder for the following reasons: Engine speed (N) and Fuel flow (F) signals are supplied by the standard aircraft transducers (see Table 1) as pulse trains[2] with repetition rate proportional to the measurand. It is possible to convert the varying frequency of the pulse train to an analogue voltage in a signal conditioner and deal with the result as an analogue input proportional to the instantaneous value of the parameter being measured. However consideration of the accuracy requirements of N and F favoured direct conversion of frequency to a digital form by counting the number of cycles in a fixed time interval. The counting technique results in a value which is an average for the time interval. Resolution is readily improved by increasing the sampling rate and removing progressive errors using the technique described by Fraser[2].

Configuring the recorder around a digital bus, to which a digital input provides access, allows for extension of the system, and also monitoring measurements during calibration, commissioning and maintenance.

It was decided to provide four digital channels to allow expansion from the two required for N and F.

2.6 Recording Duration

Macchi aircraft flights in the training role do not normally exceed one hour. For this reason a one hour recording duration was provided.

2.7 Sampling Rate

The rate of change of the parameters given in section 2.1 is such that a one second sample rate is more than adequate.

2.8 Accuracy and Resolution

Accuracy requirements were investigated in parallel with a review and assessment of existing data acquisition systems likely to meet the expected requirements. On the basis of a specific system proposal detailed below in Section 2.10, it was agreed to work within a system resolution of 8 bits, that is a resolution of 1 in 256.

One exception to this overall resolution requirement was Engine Speed (N) which, as a

sensitive parameter in the mathematical expressions for engine condition, required better resolution. An effective resolution of 9 bits was accomplished by scaling N so that an 8 bit counter could be filled twice per second.

2.9 Data Handling and Analysis

Since the engine monitoring system might eventually be put into service at operational bases, it was considered essential that the data medium be of a cassette type to allow ease of handling by air crew. A second essential requirement was analysis by computer to provide quick turnaround.

2.10 System Choice

An early decision was made to manufacture a prototype system within the Laboratories. A market survey of data acquisition systems indicated that existing equipment was unacceptable for one or more of the following reasons: too expensive, too large/heavy, unnecessarily sophisticated, or not designed for an airborne environment. A British and a Canadian system were noted as possibilities but they were both still in the development stage.

A VGH recorder[1] developed in the Laboratories appeared to provide a suitable basis for the engine condition monitoring system. It fulfilled many of the requirements; in particular, it incorporated a special digital encoding system which permitted the use of a consumer grade cassette tape recorder, but it was limited in having only four channels and no provision for digital input. The particular features of the VGH recorder which made it attractive as a basis for the engine health recorder are:

(i) Designed for airborne use.
(ii) Directly powered by the aircraft battery (a nominal 28 V).
(iii) Small, light and already environmentally tested.
(iv) Uses a Philips 3302 cassette recorder for data storage which is inexpensive and easy to use.
(v) The mechanical drawings for the VGH recorder were available and could be used with only minor modifications.
(vi) The power supply module could be used unchanged.
(vii) The printed circuit card which provided timing and control signals and the recording code could be used with a changed programme in its programmable read only memory (PROM).

The prototype recorder developed, known as the 16 CAD recorder (16 Channel Analogue and Digital recorder) was accordingly based on the VGH recorder, and was designed to conform with all the requirements outlined in Sections 2.1 to 2.9.

3. GENERAL DESCRIPTION OF SYSTEM

A block schema of the total system is provided in Figure 2. The system has two parts, the airborne sub-system and the ground sub-system. Information is transferred between these on a Philips standard cassette.

3.1 Aircraft Sub-system

The components of the aircraft sub-system can be grouped in three categories:

(i) Transducers which sense the variables to be recorded and provide related electrical signals.
(ii) Signal conditioners, which take the electrical signals from the transducers and by filtering, amplification or pulse counting provide suitable signals for the data recorder.
(iii) The data recorder which in this case in the 16 CAD recorder, described in detail in Section 4.

Details pertaining to the selection of analogue transducers are given by Edwards[5].

The pulse rate transducers for engine speed and fuel flow are standard aircraft units. The signal conditioning required for these is described by Fraser[2].

Krieser[3] has described the signal conditioning required for the inlet and exhaust gas temperatures.

3.1.1 The 16 CAD Recorder as part of the Sub-system

The 16 CAD recorder is a small light and robust data recorder which accepts up to 12 analogue inputs and 4 digital inputs. A special encoding technique enables an inexpensive consumer-quality cassette recorder to be used. The sampling rates and sampling order are programmed on a Programmable Read Only Memory. Analogue inputs are multiplexed and digitized to 10 bit words of which the 8 most significant bits are encoded and recorded. The recorder is configured around a two way digital data bus which, in addition to accepting direct digital inputs, allows a digital display monitor to display the contents of the bus (the full 10 bits) for calibration and general maintenance. The 16 CAD recorder is the front unit in the photograph Figure 1. A block schema of this unit is shown in Figure 3(*a*).

Table 1 lists the 16 channels of the 16 CAD recorder, the variable for each allocated channel, the transducer type and a reference for details of the signal conditioning.

3.1.2 The Digital Signal Monitor

In many digital data acquisition systems it is difficult to obtain a suitable read-out of the data prior to recording. Under such circumstances, pre-flight check-out and calibration of the system housed in an aircraft can be very involved. The digital signal monitor greatly facilitates pre-flight preparations. It monitors the data bus carrying time multiplexed digital data. The desired channel address is set up, in octal, on a thumb wheel switch, and the data presented on that channel are displayed as four octal digits. A block schema of the monitor is shown in Figure 3(*b*). The 16 CAD recorder has a 10 bit data bus, only the high order eight bits are recorded, but the full 10 bits can be monitored. This proves very useful for accurate bench calibration of the system. To allow ease of comparison of the eight bit numbers recorded with the 10 bit numbers displayed, the first three octal digits displayed represent the 8 bits recorded, the least significant two bits are allowed to form an octal fraction in the last display. The display range is thus $000 \cdot 0_{(8)}$ through to $377 \cdot 6_{(8)}$, where only the even octal fractions occur, the least significant bit of the fractional display always being zero.

Further details on the display are given by Drazenovic[4].

3.2 Ground Sub-system

The ground portion of the engine condition monitoring system is shown schematically in Figure 2. The primary purpose is to facilitate digital computer analysis and printout in a suitable format. This aspect is dealt with by Wood[6, 7].

While direct computer entry of data from cassette is possible, it is simpler to first transcribe the recorded data onto a standard half inch industry compatible seven track magnetic tape.

In transcription, data words are written as two serial four bit bytes on the computer compatible tape. Frames of data words are grouped into records of 10 frames with standard inter-record gaps between records. Frame synchronisation is retained by writing an identifier on the two otherwise unused tracks when the first 4 bit byte of a frame is written. No attempt is made to detect drop-outs or other errors during the transcription process. Transcription is unaffected by changes in frame size or sampling format.

3.2.1 Transcription Unit

A block diagram of the transcription unit is shown in Figure 4. Recorded data cassettes are replayed on a standard audio cassette recorder and the data re-recorded on an incremental digital recorder. Signals from the replay deck are applied to a set of tone detectors and monostables which detect each tone transition. The outputs are connected to a ternary to binary decoder which reconstructs the recorded sequence of serial binary data. A clock signal for this data is obtained by "OR-ing" the outputs of the tone decoder monostables.

The binary data are assembled into four bit half words in a shift register and fed into a first in first out memory. Frame mark signals and output recorder commands are also entered into separate channels of the first in first out memory as required. Use of a first in first out memory greatly simplifies the problem of storing input data while the output recorder is writing gaps and writing out data at a rate faster than the input rate when the output recorder is writing records.

Relating the recorder control signals to the data pattern by entering control signals into the first in first out memory allows the output device timing to be made completely independent of timing signals from the data.

At the conclusion of a data record on the cassette tape the output recorder is instructed to write an end of file gap. If the data record is followed by another data record on the same cassette at a sufficiently small interval, as indicated by the reappearance of data before the gap is finished, only a single end of file gap is written. If data have not reappeared before the first gap is finished a second end of file gap is written. This feature is used to distinguish between breaks in data due to switching the recorder off and on and the conclusion of a recording period as end-of-tape.

The computer compatible tape is recorded on a Kennedy DS370RFC recorder at 556BPI with odd parity. This incremental recorder accepts logic levels of zero volts for binary 0 and minus six volts for binary 1. The Interface Box (Fig. 2) allows the Kennedy recorder to communicate with standard transistor-transistor logic levels.

3.2.2 Output Signal Monitor for Transcription Unit

This signal monitor complements the digital display monitor used with the airborne subsystem. The output signal monitor takes the seven track format data prepared for the Kennedy recorder and displays the data recorded for any of the 22 sample epochs of the 16 CAD recorder data frame. This selection is made by dialling decimal 0 through to 21 on a thumbwheel switch. Channel address cannot be used because this information is not present in the recorded data. Channel address can be selected by referring to Table 2.

As a quick check of the data during transcription, channels 9, 10 and 11 can be monitored by dialling up sample numbers 7, 12 and 19 respectively. These channels have calibration signals with the expected readings as follows:

Sample No. (Decimal)	Channel No. (Decimal)	Display (Octal)
7	9	200
12	10	372
19	11	005

The detailed operation and circuit of this monitor may be found in Appendix 3.

4. 16 CAD RECORDER—DETAILED DESCRIPTION

Apart from transducers and their associated signal conditioners, the major component of the airborne sub-system is the sixteen channel analogue and digital (16 CAD) recorder.

As manufactured in the laboratories, the recorder had overall dimensions of $30 \times 13 \times 12$ cm and weighed 7·7 kg. While it was developed to serve a specific application, it is suitable for a variety of aircraft, ship and automotive data logging tasks.

The assembly (see Fig. 3(*a*)) is comprised essentially of a low cost audio magnetic tape recorder and 5 electronic units designated power supply, crystal clock, data recording, analogue data acquisition, and analogue calibrator. These units are contained on 5 printed circuit cards known for convenience as power supply cards (2), clock card, digital card and analogue card. The function and design of each unit is described in detail in the following sections.

The central element of the 16 CAD Recorder is the inexpensive magnetic tape recorder, which is used unmodified to record digital data bits on a standard cassette by means of a special ternary tone scheme which is described in Section 4.3.1 and Appendix 1.

4.1 Power Supply

The power supply is a separable module $13 \times 7{\cdot}9 \times 5{\cdot}8$ cm which accepts power at 28 volt from the aircraft. A simplified schema is shown in Figure 5, which also lists the detailed drawings. The power supply uses a DC–DC converter to provide isolation of the various voltages required. A transformer coupled, push-pull transistor switch converts the 28 volt input to an AC output. The transformer has three separate centre tapped secondaries. The five voltage rails derived from these are required because, in addition to the ± 15 volt rails for the analogue

circuits, and the 7·5 volt cassette recorder power, the active components come from three separate families, viz. *TTL*, *MOS* and *CMOS*. The +5 volt for the *TTL* and *MOS* is derived from regulator IC1 which is energized by one centre tapped winding and full wave rectified by D5 and D6. The ±15 volt for the analogue circuits are derived from regulators IC2 and IC3 energized by the second centre tapped winding, bridge rectified by D9, D10, D11 and D12. A simple zener regulator derives the −12 volt needed to bias the *MOS* devices from the output of the −15 volt regulator. The 7·5 volt cassette recorder supply has its own regulator IC4 energized by the third centre tapped winding full wave rectified by D7 and D8.

The power supply is capable of providing power up to a maximum input current of 1·6 Amp at 28 volt. Input currents in excess of 1·6 Amp cause the transformer in the converter to saturate and oscillations to cease. Hence output power is limited.

In the present application, the actual input current at 28 volt is a total of 750 mA, of which the contributions attributable to the power requirements of the itemized units are given below:

Power supply	225 mA
Tape recorder	50 mA
Clock Card	25 mA
Digital Card	250 mA
Analogue Card	200 mA
Total	750 mA

4.2 Clock Card

A photograph of the clock card is shown in Figure 6. Figure 7 lists the detailed drawings.

4.2.1 Crystal clock

Because of the technique used for measurement of engine speed and fuel flow, a crystal controlled system clock is required in order to provide precise time intervals commensurate with the resolution of the system. Assuming use of the full 10 bits resolution (i.e. 0·05% of full scale) the time period should have one order better accuracy (0·005%).

The schema for the crystal clock is shown in Figure 7. The crystal frequency is 1296·00 kHz. The crystal is connected to a MK5009P integrated circuit which is a combined oscillator and programmable frequency divider. The frequency of 1296 kHz is divided by 3600 to give the 360 Hz required by the digital card. The change in frequency of the nominal 360 Hz was measured over a temperature range of −20°C to +60°C and the results are shown in Figure 7. It is seen from the graph that the frequency changes by 0·0015% over the given temperature range.

4.2.2 Other Functions Performed on the Clock Card

The clock card as can be seen from the photograph (Fig. 6) is not highly utilized with respect to available card area. It was convenient to place on this card two unrelated functions.

(i) The Command To Convert (*CTC*) Buffer and the Channel Address Buffers. These buffers are necessary when a general two-way digital bus is taken to the "outside world". The buffers allow the *CTC* and the channel address lines a "fan out" of 30 so they may drive external devices via the digital input/output port. The channel addresses are buffered by 7408 *TTL AND* gates, so no logical inversion occurs. The *CTC* however is inverted by a 7400 *TTL NAND* gate as a matter of hardware convenience in the Engine Speed and Fuel Flow Signal Conditioner[2].

(ii) The Analogue Calibrator, while this is on the card, is more appropriately dealt with under Section 4.4 Analogue Card.

4.3 Digital Card

The Digital Card controls interrogation of acquisition devices connected to the digital bus, accepts the data taken from the bus, formats the data, and encodes it into ternary FSK Figure 8 is a photograph of the card.

4.3.1 Ternary Frequency Shift Keying

This coding method is due to Patterson[1] who has described its development.

Three frequencies are used f_H (5·06 kHz), f_M (3·38 kHz), f_L (2·25 kHz). The spacing of the frequencies is chosen so that variations of ±20% from the nominal value may occur without ambiguity. The tape transport speed variation does not exceed ±20% under the acceleration conditions encountered.

In operation, f_H is assumed to exist prior to the start of a record. Referring to the state diagram for the code (Fig. 9) it is seen that a string of ones is encoded as a cyclic $f_L f_M f_H f_L f_M f_H f_L f_M$. A string of zeros is encoded as $f_M f_L f_H f_M f_L f_H f_M f_L$. A frequency change occurs at each bit change, enabling a bit clock to be simply extracted from the recorded tones. Appendix 1 gives a detailed analysis of the tone encoder employed on the digital card.

4.3.2 Format of Record on Tape

The data are recorded in frames of one second. To achieve frame synchronization a gap of four bits duration is inserted in each frame.

Bit synchronism is obtained from the self-clocking properties of the ternary FSK code.

There are 22 words each eight bits long recorded in one second. Allowing for a four bit gap, this creates a frame 180 bits in length.

Each word is recorded most significant bit first. In offset binary, used for analogue variables, the *MSB* is the sign bit.

4.3.3 Data Sample Rate

The digital card controls the data sample rate. For convenience in later analysis, it is required that samples from any given channel be taken at equal time intervals. If more than one sample per second is required per channel, then the more factors there are in the total number of samples per second, the better. In this respect the 16 CAD recorder's 22 samples per second cannot be considered particularly suitable. The situation is improved by providing irregular sampling rates. Specifically, 20 samples are taken at $\frac{1}{20}$th second, and two extra samples (the second and third) fit between the first and fourth samples at $\frac{1}{60}$th second intervals. This sample pattern restricts the second and third samples to channels which are sampled once per second but markedly improves the flexibility of the other 20 as can be seen in Section 4.3.6 Channel Sample Sequence.

The data sampling is controlled by the Command To Convert signal which is shown in Figure 12 for a complete one second frame.

4.3.4 Data Flow on Digital Card

A simplified schema of the Digital Card is given in Figure 10. The waveforms generated on the card are shown in Figure 11. Sections 4.3.2 and 4.3.3 described the data output and input formats respectively. This section describes how the hardware accomplishes the required formats.

A four bit channel address and a *CTC* are sent to the digital bus. After 2·78 milliseconds, a four bit byte multiplexer, controlled by waveform SI/2, selects the four most significant data lines and waveform SI (Shift In) shifts the high order byte into a four bit wide First In First Out (FIFO) memory. SI/2 now selects the four least significant data lines (of the eight data lines recorded) and SI shifts the low order byte into the FIFO. Then, 2·78 milliseconds after completion of this second SI, a Shift Out (SO) pulse shifts the first byte out of the FIFO, into a parallel-in serial-out shift register. The FIFO, with its independent SI and SO controls, provides the buffer memory which allows the different speeds of sampling and recording to be matched. The 180 Hz Bit Clock shifts the serialized data into the ternary encoder, where the appropriate tones are generated (Section 4.3.1 and Appendix 1). The ternary FSK tones pass through the gap switch, which under control of the Gap Control signal, inhibits the passage of tone during the frame synchronizing gap. The tone signal leaves the gap switch and enters the normal audio input of the cassette recorder.

It is important that all data acquisition devices accessed by the digital bus be capable of responding within the 2·78 milliseconds between the CTC and the SI pulses. In general this time is more than adequate.

4.3.5 Read Only Memory Control

The format of the control signals and the channel sample sequence are determined by a Read Only Memory (ROM). The ROM has a five bit input address which allows access to 32 words of eight bits in length. The ROM programme is given in Table 2. The first four bits are control bits and the last four bits provide the addresses of the 16 channels. The ROM address is also the sample number of the 22 sample frame (the last 10 ROM addresses are not accessed). The functions of the 8 bits in the ROM programme are now defined:

$B_0 = 1$ Selects a data sample rate of $\frac{1}{60}$th second.

$B_0 = 0$ Selects a data sample rate of $\frac{1}{20}$th second.

$B_1 = 1$ Resets the Bit Clock counter and inhibits readout from the FIFO during an inter-frame gap.

B_2 A $1 \rightarrow 0$ transition resets the FIFO prior to the first SI pulse of the one second frame.

$B_3 = 0$ Causes the ROM address counter to be reset on the next counter clock pulse (SI/2).

B_4 Least significant bit of the channel address.

B_5 Channel address bit.

B_6 Channel address bit.

B_7 Most significant bit of the channel address.

4.3.6 Channel Sample Sequence

The channel sequence is programmed in the ROM (see Table 2). Although for the present application six analogue channels and two digital channels were required, a sequence involving all 16 channels was devised. Since 22 samples are taken in one second it is possible to sample six of the 16 channels twice per second. The arrangement allows for the following:

(i) Channels 0, 1, 2, 3, 4, 5, 10, 11, 13, 15, are sampled once per second.

(ii) Channels 6, 7, 8, 9, 12, 14 are sampled twice per second.

Samples 1 and 2 (see Table 2) which are taken at $\frac{1}{60}$th sec are interpolated in an evenly spaced $\frac{1}{20}$th sec sample pattern; they must therefore be allocated to channels for which only one sample per second is required. Channel addresses 1 and 2 have been chosen.

Engine speed N is a digital input which must be sampled twice per second for correct scaling and resolution[2]. N is given channel address 12. Channel 14 which is not used in this application is placed in the sampling cycle midway between channel 12 samples so that a device recognizing addresses 12 or 14 would be sampled four times per second. Digital samples 13 and 15 are sampled once per second but so placed that a device recognizing addresses 13 or 15 would be sampled twice per second. Address 13 is allocated to fuel flow (F).

Analogue channels are allocated addresses 0 to 11.

Digital channels are allocated addresses 12 to 15.

Table 1 lists channel addresses and respective variables for each.

4.3.7 Generation of Wave-forms

A description of the sequence in which the Digital Card wave-forms are generated is now given. This description may be read in conjunction with Figure 10, Figure 11 and Table 2.

The crystal-derived 360 Hz frequency, received from the clock card is divided by three to 120 Hz and by three again to 40 Hz. $B_0 = 1$ for the first three ROM addresses and six cycles of 120 Hz are selected as the initial FIFO Shift In (SI) pulses. SI is divided in frequency by two, giving SI/2 which serves as the ROM Address Counter input as well as the High Byte/Low Byte selector. At ROM address one, $B_1 = 1$, $\overline{B_1 \cdot \mathrm{SI}/2}$ resets the counter generating the 180 Hz Bit Clock and derived waveforms. $\overline{B_1 \cdot \mathrm{SI}/2}$ also sets the Gap Control Latch.

The 360 Hz is also divided by two giving the 180 Hz Bit Clock which clocks the data serially through the Ternary Encoder. The 180 Hz is divided by two to 90 Hz and again to 45 Hz. The

90 Hz and 45 Hz are "AND-ed" giving the Byte control or FIFO Shift Out (SO). $B_1 = 1$ inhibits this waveform during the four bit gap. Thus 44 SO pulses are generated in a one second frame, one for each of the four bit bytes the 22 data words are multiplexed into to fit the four bit wide FIFO. The first S0 after the interframe gap resets the gap control latch.

For ROM address three on, $B_0 = 0$ so SI proceeds at 40 Hz and SI/2 at 20 Hz. Sampling continues at this rate until the ROM address reaches 21. B_3 changes from 1 to 0 and on the next count, the ROM address counter is reset to zero. A frame has now been completed.

As the ROM address goes from 21 to 0, B_2 has a 1 to 0 transition, $\overline{B_2} \cdot \overline{SO}$ generates a short transition which resets the FIFO prior to the first SO of the next frame. The Command To Convert waveform is generated in a latch set by a negative transition of SI/2 and reset by a negative transition on the 180 Hz.

4.4 Analogue Card

The analogue card accepts the 12 analogue inputs, multiplexes them in a sequence determined by the channel addresses transmitted from the digital card by the digital bus and converts the analogue samples taken to 10 bit offset binary words. These words are transmitted to the digital bus for recording by the digital card and may be monitored visually.

A photograph of the analogue card is given in Figure 13. A simplified schema is given in Figure 14 where the detailed drawing numbers are also listed. The operation of the card is described in the following sections.

4.4.1 Channel Interrogation Circuitry

The interrogating waveforms, which are generated on the digital card, consist of the four bits of channel address and the CTC. One complete data frame of these waveforms is shown in Figure 12. The binary code for the channel address is first converted from nominal *TTL* levels to levels appropriate for operating the *CMOS* analogue gates. This is done by an LM324 quad amplifier. The four amplifiers are operated open loop in a non-inverting configuration. A voltage divider provides an offset voltage to the inverting inputs so that zero volt in gives $-6{\cdot}5$ volt out. An input of $+5$ volt gives $+6{\cdot}5$ volt out.

The address is now decoded by an MM74C154 *CMOS* four bit to 16 line decoder. Logic level low is true for the outputs of this device so outputs zero to eleven are inverted by MM74C04 *CMOS* inverters before driving the MM5616 analogue gates.

4.4.2 Analogue Multiplexer

The analogue multiplexer time-multiplexes 12 channels of differentially fed analogue signals. The analogue gates used are *CMOS* MM5616 quad gates. To minimise mismatch between the *ON* resistances of different gates, the two gates for a differential pair are chosen from the same package.

The differential amplifier used to buffer the output of the analogue gates is an LM308. The low offsets and drifts of this amplifier allowed the operational resistors to be selected at a nominal 100 kΩ. The resistors were matched to within $\pm 0{\cdot}005\%$ on a resistance bridge and as a consequence no trimming resistors were required.

The Common Mode Rejection Ratio of the amplifier output with respect to the input of the analogue gates has been measured as 80dB to a signal frequency of 10 Hertz and is 74dB at 100 Hertz. The channel cross-talk has been measured as 75dB below the full scale signal at 100 Hertz and 66dB below at 400 Hertz. These figures are quite acceptable for a system with a maximum sampling rate of 22 samples per second and a resolution of 10 bits. Complete curves for *CMRR* and cross-talk versus frequency are given in Figures 15 and 16 respectively.

4.4.3 Analogue to Digital Conversion

Analogue to digital conversion is performed by an "Analog Devices" ADC10Z, a 10 bit successive approximation converter with a maximum conversion time of 20 μs. The ADC gain is set by RV_1 and RV_2 sets the zero. The digital output is *TTL* compatible 10 bit offset binary. Links between pins 16 and 19 or 21 and 22, combined with selection of values of RV_1 allow

the following input voltage ranges to be selected: 0–5 volt, ±5 volt, 0–10 volt, ±10 volt. The range selected for this application is ±5 volt.

The ADC10Z has no inbuilt means for accessing a shared data bus. Ten tristate buffers provide this access. The buffers are disabled when channel address bits CA4 and CA8 (Fig. 12) are high, i.e. the channel address is 12 or greater. Channel addresses of 12 or greater are allocated to direct digital inputs.

It is worth noting that two otherwise unused tristate buffers have been configured to form an unconventional AND logic function for this purpose. It is possible to similarly configure mixes of DM8093 and DM8094 gates to provide all the common logic gate functions including Exclusive OR.

4.4.4 Analogue Calibration Reference

Although this unit is physically on the Clock Card, its function is best described in association with the Analogue Card. The circuit for the calibration reference is given in Figure 17. Four LM113 reference diodes are connected in series to provide a voltage reference of 4·8079 volt at 20° Celsius. The four diodes were selected for minimum temperature coefficient from a batch of 20. The variation of voltage of the combined chain against temperature is given in the table below:

Temp. °C	Voltage
60	4·8050
40	4·8069
20	4·8079
0	4·8075
−20	4·8057

The reference voltage and zero volts are brought out on spare pins of the analogue input connector 2J5. A mating connector 2P5 is wired so that three otherwise unused analogue channels receive the voltages shown in the following table.

Channel	Input Voltage	Recorded Digits (Octal)	Monitored Digits (Octal)
9	0·0000	200	200·0
10	+4·8079	372	372·6
11	−4·8079	005	005·2

The calibration voltage has proved a very useful check on the integrity of the overall system. Channels 9, 10 and 11 are readily monitored prior to a flight, on the aircraft and during transcription. The recorded values proved so reliable that they could have been used by analysis software to automatically adjust offset and scaling.

4.5 Digital Bus and Its Protocol

Much of the following information is given elsewhere in this report but for ease of reading a unified description is presented here. The configuring of the 16 CAD recorder around a two-way digital bus was a direct consequence of the decision to measure fuel flow and engine speed digitally. The bus adds greatly to the flexibility of the 16 CAD recorder as a general purpose instrument; it also makes the operation of the recorder on a long term project very much easier. Practical experience has demonstrated that if a digital bus exists, it is essential to have access to it and a means of selecting and capturing for display any desired phase of its operation. This claim is evidenced by Sections 3.1.2, 4.4.4 and Appendix 2 (checkout of the Recording Card Functions Using the Digital Input) of this Report.

The bus is accessed by means of a 19 pin Cannon *KPT* connector. Figure A2–1 lists the connector pins and the bus functions. There are 10 lines for digital data, four lines for channel address, a CTC line, a common, a +5 volt line and two spare lines. The CTC available on the connector is the logical inversion of that taken to the analogue card.

The bus protocol is very simple: a channel address is transmitted along with a CTC pulse, the CTC is used as a general interrogation command. Upon a data acquisition device receiving its appropriate address and a CTC, acquisition is initiated and the device is connected to the bus by enabling tristate buffers. These activities are required to be completed within 2·78 milliseconds, at which time the Digital Card will accept whatever is presented to the bus.

Many two way data transmission protocols require that all the devices accessing a communication link have a unique address. In this application it is desirable that all the available addresses be input channel addresses. This apparent constraint greatly simplifies the bus protocol and the hardware required to implement it.

In the present configuration there are two receiving devices, the Digital Card and the Digital Signal Monitor and they have no addresses allocated. The Digital Card simply accepts all data offered to it 2·78 milliseconds after the CTC while the Digital Signal Monitor selectively accepts data from a given address by logically testing the address lines.

5. OPERATIONAL EXPERIENCE

The equipment described was installed in a RAAF Macchi No. A7–048 and flown by ARDU between November 1974 and March 1976 during which time it operated for many hundreds of hours and the reliability of various aspects of the system was established. Since March 1976 the equipment, installed in Macchi A7–048, has been flown on a normal operational basis from East Sale Air Base.

Operational experience has shown that although the system has proved quite workable the present transcription unit constitutes a bottleneck in the processing of data because the technique is slow, cumbersome and occasionally unreliable. A proposal to replace this hardware by a microprocessor based unit, controlled by suitable software, is now being considered. The main benefits will be greatly increased speed, enhanced flexibility of operation and optionally the ability to convey the data directly to a computer without the need for intervening tape storage.

Practical use of the 16 CAD recorder in aircraft has also shown the need for protecting the input of the analogue multiplexer against over-voltage. Hence the analogue multiplexer was replaced with a device which is protected against higher input voltage overloads. Several associated circuit changes had the effect of improving the Common Mode Rejection Ratio.

Analysis of the measurements made in the engine condition monitoring programme have indicated the need for greater resolution in selected parameters. A modification is now under development to upgrade the recorded resolution on four analogue channels.

Details of all the above changes will be reported in due course, when they have been incorporated and operationally tested.

6. CONCLUSIONS

The feasibility of designing and constructing a useful, compact, low cost and robust analogue and digital data recording system has been demonstrated.

The novel features of the system described in this report have ensured that the specified requirements of resolution and accuracy have been adequately achieved.

As a result of operational experience, several detailed improvements have been indicated; nevertheless the basic design has potential applications for many data acquisition tasks involving severe environmental stresses.

ACKNOWLEDGMENTS

The author would like to acknowledge the contributions made and the helpful cooperation given by the following individuals and organizations:

Mr A. K. Patterson and his colleagues in Structures Division who designed and built the VGH recorders and their transcription unit.

Engineering Facilities for the mechanical design of the 16 CAD recorder, and its manufacture.

Mr R. W. Jackson who jointly bench calibrated the 16 CAD recorder with the transducers used.

Mr K. F. Fraser who devised the output signal monitor for the transcription unit and with whom close discussions on the best method for measuring engine speed inspired the architecture of the 16 CAD recorder.

REFERENCES

1. A. K. Patterson, M. T. Adams — Two Low Cost Aircraft Data Acquisition Systems. I.I.C.A. National Symposium 1975.
2. K. F. Fraser — Aircraft Engine Speed and Fuel Flow Signal Conditioner with Digital Output. A.R.L./M.E. Note 354, November 1974.
3. U. R. Krieser — Conditioner For Use in the Acquisition of Aircraft Temperature Data. (to be published).
4. B. Drazenovic — Digital Display Monitor for Pre-Flight Checking and Calibration of Aircraft Digital Data Acquisition System. A.R.L./M.E. Tech. Memo. 365, December 1974.
5. D. H. Edwards — Instrumentation of a Macchi Aircraft for an Engine Health Monitoring Programme. (to be published).
6. F. J. P. Wood — Data Recording for Viper Engine Health Monitoring. A.R.L./Mech. Eng. Tech. Memo. 377, May 1976.
7. F. J. P. Wood — Data Recording for Viper Engine Health Monitoring (Part 2). A.R.L./Mech. Eng. Tech. Memo. 385, September 1977.

TABLE 1

Digital Data Acquisition System for Engine Condition Monitoring: Channel Addresses, Variables, Transducers and Signal Conditioning

Channel No.	Variable	Symbol	Transducer	Signal Conditioning
0	Ambient Pitot Pressure	P_t	National LX1600	Reference[1]
1	Ambient Static Pressure	P_s	National LX1600	Reference[1]
2	Engine Intake Total Pressure	P_1	Kistler 314A S/N 780	Included with Transducer
3	Exhaust Gas Total Pressure	P_4	Kistler 314A S/N 789	Included with Transducer
4	Engine Intake Total Temperature	T_1	Rosemount 100Ω at 0°C	Reference[3]
5	Exhaust Gas Total Temperature	T_4	Rosemount E32026 SA1701 Range 0–1000°C	Reference[3]
6	Unused			
7	Unused			
8	Unused			
9	Zero Calibration			
10	+Calibration [+4·8079 V at 20°C]			Figure 17
11	−Calibration [−4·8079 V at 20°C]			Figure 17
12	Engine RPM	N	Smiths KGA0701 Tacho-generator	Reference[2]
13	Fuel Flow Rate	F	Faure Herman RCM128PA Rotating impeller type	Reference[2]
14	Unused			
15	Unused			

Channels 0 to 11 accept Analogue Signals between nominal ±5 volts.
Channels 12 to 15 accept an 8 bit parallel word after an appropriate address and read command have been issued.

TABLE 2
16 CAD Recorder ROM Programme

P_1

Sample No.	Channel No.	ROM Address					ROM Program							
							Control Bits				Channel Addr.			
		A_0	A_1	A_2	A_3	A_4	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7
0	0	0	0	0	0	0	1	0	0	1	0	0	0	0
1	1	0	0	0	0	1	1	1	1	1	1	0	0	0
2	2	0	0	0	1	0	1	0	1	1	0	1	0	0
3	12	0	0	0	1	1	0	0	1	1	0	0	1	1
4	6	0	0	1	0	0	0	0	1	1	0	1	1	0
5	7	0	0	1	0	1	0	0	1	1	1	1	1	0
6	8	0	0	1	1	0	0	0	1	1	0	0	0	1
7	9	0	0	1	1	1	0	0	1	1	1	0	0	1
8	14	0	1	0	0	0	0	0	1	1	0	1	1	1
9	3	0	1	0	0	1	0	0	1	1	1	1	0	0
10	4	0	1	0	1	0	0	0	1	1	0	0	1	0
11	13	0	1	0	1	1	0	0	1	1	1	0	1	1
12	10	0	1	1	0	0	0	0	1	1	0	1	0	1
13	12	0	1	1	0	1	0	0	1	1	0	0	1	1
14	6	0	1	1	1	0	0	0	1	1	0	1	1	0
15	7	0	1	1	1	1	0	0	1	1	1	1	1	0
16	8	1	0	0	0	0	0	0	1	1	0	0	0	1
17	9	1	0	0	0	1	0	0	1	1	1	0	0	1
18	14	1	0	0	1	0	0	0	1	1	0	1	1	1
19	11	1	0	0	1	1	0	0	1	1	1	1	0	1
20	5	1	0	1	0	0	0	0	1	1	1	0	1	0
21	15	1	0	1	0	1	0	0	1	0	1	1	1	1

B_0	1	selects $\frac{1}{60}$ s between Samples: 0 selects $\frac{1}{20}$ s
B_1	1	resets bit clock divider and prevents readout from FIFO
B_2	1→0	transition resets FIFO
B_3	0	causes ROM address counter to be reset on next counter clock pulse
B_4		Least significant bit of channel address
B_5		
B_6		
B_7		Most significant bit of channel address.

TABLE 3
Calibration of Pressure Transducers

Pressure kPa	Octal Output For Channel: 0	1	2	3
206·988			377·0	377·2
193·198			356·0	356·2
179·408			335·2	335·2
165·618			314·2	314·2
158·723	375·2		304·0	304·0
151·828	362·4		273·4	273·4
138·038	334·0		252·6	252·4
124·248	304·4		231·6	231·4
110·458	254·2	377·4	211·0	210·4
100·115	232·0	350·6	174·0	173·6
86·325	177·4	311·0	153·2	152·6
72·535	144·6	251·2	132·4	131·4
55·298	101·6	201·2	105·2	104·4
41·508	045·2	141·2	064·2	063·4
27·718	010·2	101·0	043·4	042·4
20·823		061·0	032·6	031·6
13·928		040·6	022·4	021·4
7·033		020·6	012·0	011·2

Note: The first three octal digits only are recorded. The octal fraction is provided (as read from the ten bit *A* to *D* converter) to increase the accuracy of the calibration interpolation used in the software.

TABLE 4
Calibration for Outside Air Temperature [Total]

Temperature °C	Octal Output Channel 4
−50	377·2
−40	345·6
−30	314·0
−20	263·0
−10	231·6
0	200·0
+10	147·4
+20	116·0
+30	065·0
+40	034·0
+50	002·4

Note: The first three octal digits only are recorded. The octal fraction is provided (as read from the 10 bit *A* to *D* converter) to increase the accuracy of the calibration interpolation used in the software.

TABLE 5
Jet Pipe Temperature Calibration

Degrees Celsius Jet Pipe Temp.	Octal Output Channel 5
500	371·0
600	306·2
700	223·4
750	172·2
800	141·4
900	060·4
1000	000·2

Note: The first three octal digits only are recorded. The octal fraction is provided (as read from the 10 bit *A* to *D* converter) to increase the accuracy of the calibration interpolation used in the softwave.

TABLE 6
Engine Speed Calibration

An accessory drive shaft drives the tacho-generator used for cockpit indication of engine speed. This shaft spins at 87/286 of the main shaft speed.

The three phase tacho-generator allows a pulse to be generated in the conditioning equipment for every 60° of rotation of the accessory drive shaft, that is six pulses per rotation.

The pulses generated in the conditioning equipment are summed in a counter which is sampled twice per second and reset upon being sampled. The counter has provision for retaining any tacho-pulse arriving at the moment of reset and including this pulse in the next half second's count. This results in a precise measurement of engine speed; an average speed over the half second interval, not an instantaneous speed.

To improve resolution, the average speed over a one second interval can be counted, in which case the two half second readings MUST be added. Neglecting gross malfunctioning, Engine Speed readings totalized over a long period with respect to one second, should be accurate to within 0·002%.

The calculation for engine speed is:

$$\text{Engine revolutions per interval} = \frac{286}{87} \times \frac{\text{Pulses per interval}}{6\ \text{(Pulses per rev.)}}$$

$$\text{Revs per sec} = \frac{286}{87} \times \frac{\text{(First sample count + Second sample count)}}{6}$$

$$\text{RPM} = \frac{2860}{87} \times \text{(First sample count + Second sample count)}$$

TABLE 7
Fuel Flow Calibration

Fuel Flow Channel 13.

Channel 13 is sampled once per second.

The fuel flow factor is:

128 pulses per pound of fuel

The fuel flow range of the sensor is 160 to 4000 pounds per hour, but the range of interest for the present application is 500 to 3500 pounds per hour.

APPENDIX 1

Analysis of the Ternary Encoder.

The operation is best understood by beginning at the last 4 bit byte of a one second frame. Referring to the waveforms and schema of Figure A1–1, the last byte of a frame is shifted out of the FIFO into the parallel in serial out shift register. Following this the FIFO reset pulse clears and re-initiates the FIFO. The four bits of the last byte are duly shifted out of the shift register by the bit clock and encoded. The shift register now contains all zeros.

The Gap FF is now set and $\overline{\text{Gap FF}}$, on the direct clear of the encoding FF's hold y_1, y_2 at zero for the duration of the gap.

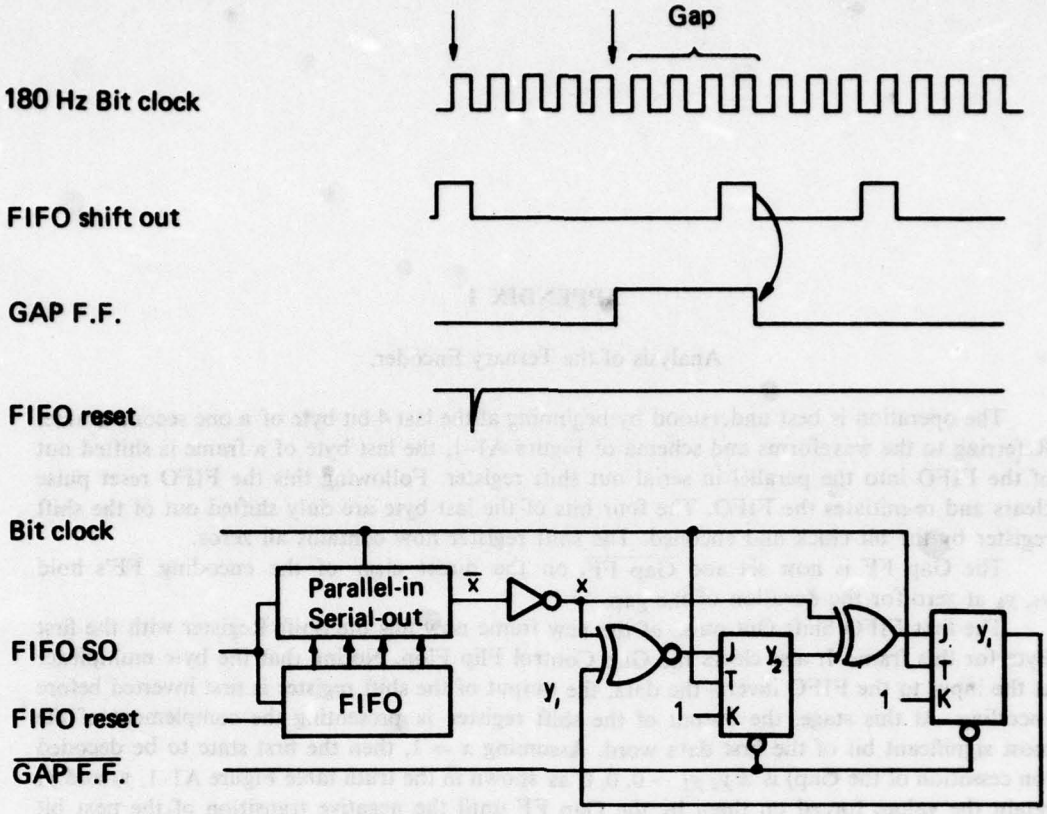
The first FIFO Shift Out pulse of the new frame now fills the Shift Register with the first Byte for this frame. It also clears the Gap Control Flip Flop. Noting that the byte multiplexer at the input to the FIFO inverts the data, the output of the shift register is first inverted before encoding. At this stage, the output of the shift register is presenting the complement of the most significant bit of the first data word. Assuming $x = 1$, then the first state to be decoded (on cessation of the Gap) is $\bar{x}\, y_2\, y_1 \rightarrow 0, 0, 0$ as shown in the truth table Figure A1–1, y_2 and y_1 retain the values forced on them by the Gap FF until the negative transition of the next bit clock pulse. Since it is assumed that f_H has been generated during the gap, and $x = 1$ then it follows, referring to Figure 9 that f_L be generated. The truth table of the output logic show that this is so, since a '0' on $\overline{f_L}$ activates f_L on the tone generator. If $x = 1$ for the next three bits then the sequence shown in the truth table for $\bar{x}\, y_2\, y_1$ epochs $t_1 \rightarrow t_4$ is generated. The output logic truth table shows that the appropriate frequencies are generated.

If $x = 0$ following a gap then from Figure 9, f_M is the first frequency to be generated and the truth table indicates that this is so. Allowing $x = 0$ for the next 3 bit clock pulses the sequence generated is shown in the rest of the truth table epochs $t_4' \rightarrow t_7$ and the output logic generates the appropriate frequencies in accordance with Figure 9.

One difficulty exists with this description; it is based on the assumption that f_H is generated during the gap. In fact if the shift register has been emptied and is at zero, then since $\overline{\text{Gap FF}}$ causes $y_2 = 0$ and $y_1 = 0$ then f_L is generated, an anomaly with respect to the "rules".

If $\bar{x} = 1$ during a gap due to false start up then f_M is generated.

It is also to be noted that if y_2, y_1 start up as 1, 1 then irrespective of the data x, f_H will be generated. Also irrespective of x, the next state for y_2, y_1 is 0, 0.



	x = 0	x = 1
$\bar{f}_H = \overline{\bar{x}y_1} \cdot \overline{xy_2}$	$\bar{y}_1$	$\bar{y}_2$
$\bar{f}_M = \overline{\overline{x \oplus y_1} \cdot y_2}$	$y_1 + y_2$	$\bar{y}_1 + y_2$
$\bar{f}_L = \overline{\overline{x \oplus y_2} \cdot y_1}$	$y_1 + \bar{y}_2$	$y_1 + y_2$

	$\bar{x}$	y_2	y_1	$\bar{f}_L$	$\bar{f}_M$	$\bar{f}_H$	EPOCH	
t1	0	0	0	0	1	1	t1	
t2	0	0	1	1	0	1	t2	
t3	0	1	0	1	1	0	t3	
t4	0	0	0	0	1	1	t4	
t4′	1	0	0	1	0	1	t4′	
t5	1	1	0	0	1	1	t5	
t6	1	0	1	1	1	0	t6	
t7	1	0	0	1	0	1	t7	
	0	1	1	1	1	0		Possible false startup conditions
	1	1	1	1	1	0		

FIG. A1-1. 16 CAD RECORDER TERNARY ENCODING LOGIC

APPENDIX 2

Checkout of the Recording Card functions using the Digital Input.

Test signals of known word composition are generated to check the behaviour of the recording card. These are applied to the digital bus via the 19 Pin connector digital inpu utput. THE ANALOGUE CARD IS REMOVED FOR THESE TESTS.

Three forms of test data have been used:

1. *Data Consisting of Repetitive 8 Bit Words the Composition of which is Switch Selectable.*

The test unit has been manufactured as an aluminium box fitted with a 3 digit thumbwheel switch which selects the octal code desired. An integral cable is terminated with a mating 19 pin connector. Data in the range 000 to 377 may be selected.

2. *Data Consisting of the Four Bit Channel Address.*

Two test connectors have been wired to feed the channel address back as data to be recorded.

2.1 Test connector 1 feeds the address back for both the high order 4 bit byte and the low order byte. For the channel sequence used, the data generated is given in Figure A2–1. This is a full frame sequence, repeating each second.

2.2 Test connector 2 feeds the address back to the low order byte only. This does not provide as complete a test of the recording system but is useful to check the address sequencing without confusion. See Figure A2–1.

These connector circuits are given in Figure A2–1.

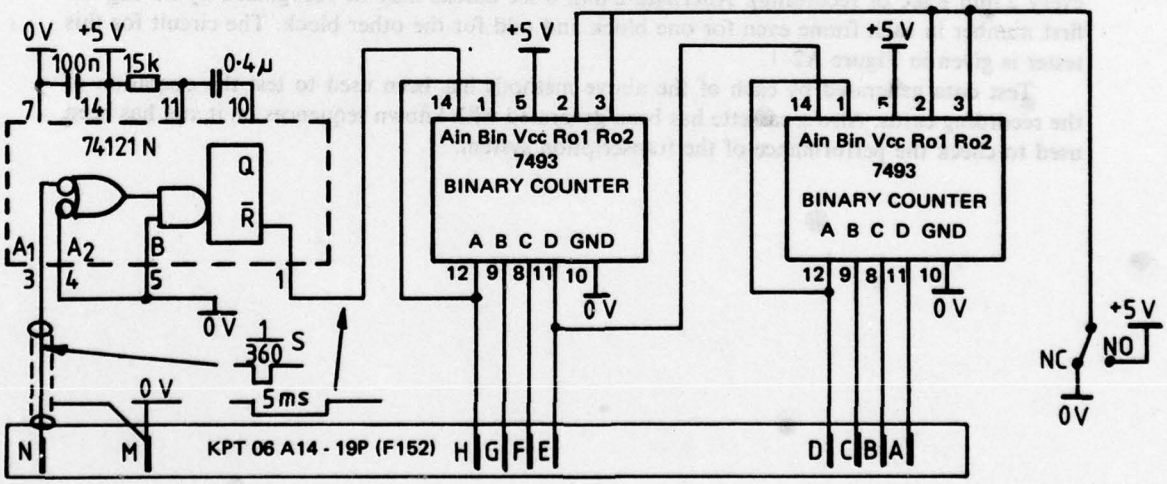
3. *Sequential Data in the Range 000 to $377_{(8)}$ which is incremented by one for Each Sample.*

In this case, consecutive 1-second frames are different (a specific channel readout will advance by $22_{(10)}$ [$26_{(8)}$] for each frame). The number pattern repeats after $128_{(10)}$ 1-second frames (i.e. every 2 min 8 sec of recording). Alternate 2 min 8 sec blocks may be recognized by having the first number in each frame even for one block and odd for the other block. The circuit for this tester is given in Figure A2–1.

Test data generated by each of the above methods has been used to test the operation of the recording cards. Also a cassette has been generated with known sequences on it and has been used to check the performance of the transcription system.

SAMPLE NO	CHANNEL ADDRESS	TEST CONNECTOR 1 SIGNAL	TEST CONNECTOR 2 SIGNAL
0	0	000	000
1	1	021	001
2	2	042	002
3	12	314	014
4	6	146	006
5	7	167	007
6	8	210	010
7	9	231	011
8	14	356	016
9	3	063	003
10	4	104	004
11	13	335	015
12	10	252	012
13	12	314	014
14	6	146	006
15	7	167	007
16	8	210	010
17	9	231	011
18	14	356	016
19	11	273	013
20	5	125	005
21	15	377	017
		OCTAL	OCTAL

BUS VARIABLE	KPT06A14 19P PIN NOS	TEST CONNECTOR 1	TEST CONNECTOR 2
Bo	A		
B1	B		
B2	C		
B3	D		
B4	E		
B5	F		
B6	G		
B7	H		
B8	J		
B9	K		
(B10)	L		
Common	M		
CTC	N		
(B11)	P		
CAB8	R		
CAB4	S		
CAB2	T		
+5V	U		
CAB1	V		
BUS FUNCTIONS		TEST CONNECTORS	



SEQUENTIAL DATA GENERATOR

FIG. A2-1. 16 CAD RECORDER DIGITAL TEST EQUIPMENT

APPENDIX 3

An Output Signal Monitor for the Transcription Unit.

Introduction

For the 16 CAD recorder, pre-and post-flight checks of the digitized data can be made using the Digital Display Monitor.

This Appendix describes a similar monitor which monitors the data conveyed from the transcription unit to the Kennedy incremental recorder. Use of the Output Signal Monitor enables a quick check of the contents of a cassette tape without undertaking computer analysis. It is not necessary to actually generate a computer compatible tape to monitor the cassette's contents.

Use of the monitor

The output signal monitor for the transcription unit has on its front panel a two bank thumbwheel switch and a three digit optical display. To display a particular recorded parameter, the channel address must be obtained from Table 1, the sample number appropriate to this channel is then obtained from Table 2 and dialled up, in decimal, on the thumbwheel switch.

The optical display will now show, in octal digits, the number recorded for that parameter in the selected sample of the one second frame. The number is updated every second. As described in the main body of the report, the analogue calibration signals can be checked using the following table.

Sample No. (Decimal)	Channel No. (Decimal)	Expected Display (Octal)
7	9	200
12	10	372
19	11	005

Operation of the circuit

The circuit for the signal monitor is given in Figure A3–1. Connector J1 joins the monitor to the output of the transcription unit (T.U.) and J_2, to the Kennedy Recorder. A Step pulse from the T.U. is delayed by 300 μs and reduced to a 300 μs length pulse by dual monostable Q9 before transmission to the Kennedy Recorder. $\bar{Q}$ of the first monostable, a low pulse of 300 μs toggles stage A of Q_7 a 4 bit binary counter, the A output defines whether the first or second 4 bit byte of a data word is being accepted from the data lines TR1 to TR4. Accordingly Quad Latch Q_4 or Q_6 accepts the byte when the Step-out pulse is generated. The A output of Q_7 also is counted by the Decade Counter Q_8 and stages B to D of the Binary Counter Q_7 to define which of the 22 samples of the one second frame is being held in the Quad Latches. The decade counter indicates the low order decimal digit of 00 to 21; the binary counter only has to deal with a high order digit range to a maximum of 3 but operates correctly up to 8. The sample count is decoded by two BCD to decimal decoders Q_1 and Q_2. Two decimal thumbwheel switches select the outputs of Q_1 and Q_2 and when both are low (true) and the second 4 bit byte has been latched and Step-out is generated, the contents of Q_4 and Q_6 are latched into the three Numeric Indicators I_1, I_2, and I_3, these being respectively the high, middle and low order octal digits representing the data word.

At the end of every one second frame, a pulse generated by the T.U. on TR5 resets the sample counter.

Every 10 seconds the T.U. generates a one second gap which is converted to a 40 ms pulse by monostable Q_{10} and displayed on the *EOR LED* as well as going to the Kennedy recorder.

Every time the tone ceases for more than four bits' duration, the T.U. generates an *EOF* pulse which is stretched to 0·9 s, displayed on the *EOF LED* and transmitted to the Kennedy recorder.

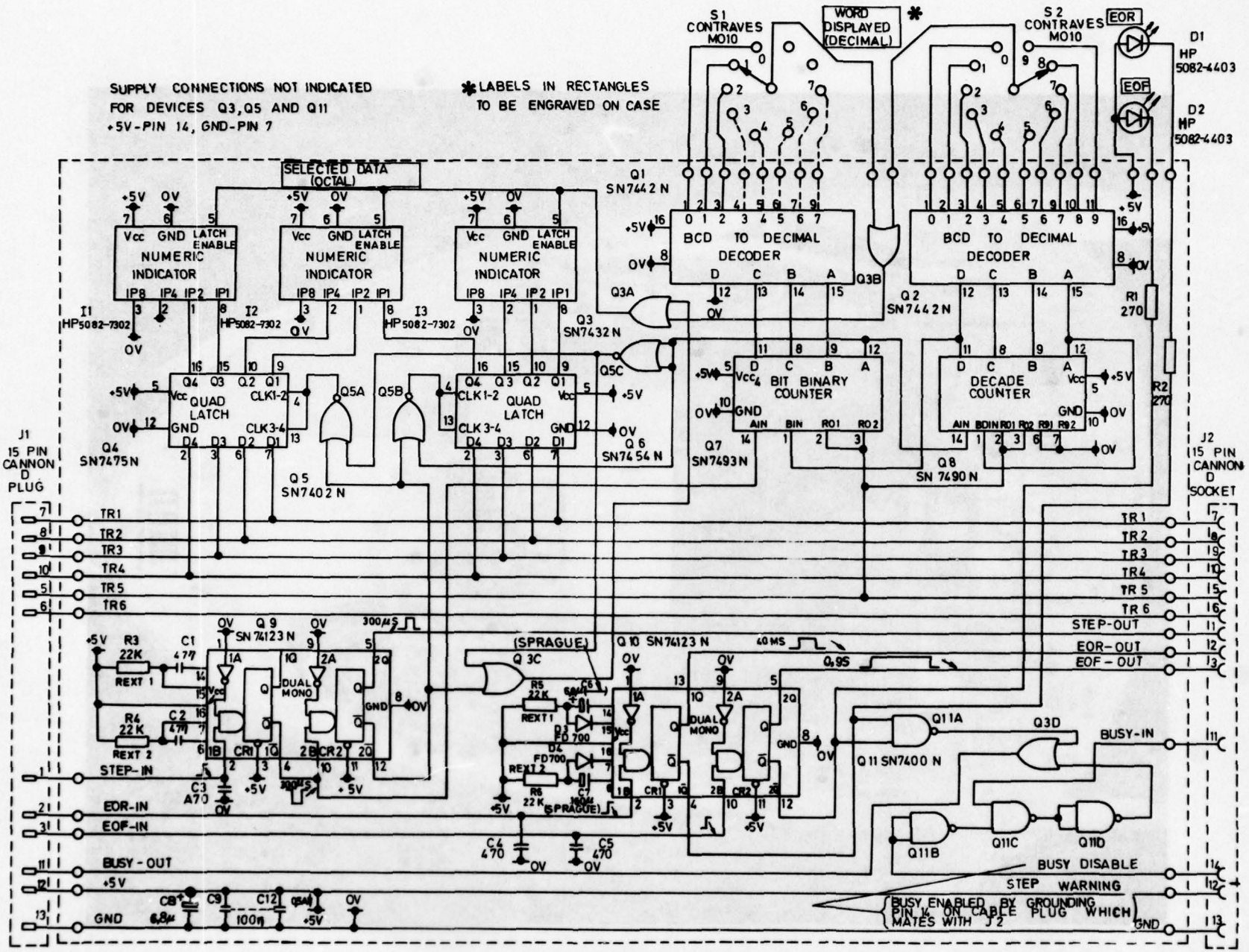


FIG. A3-1. OUTPUT SIGNAL MONITOR FOR TRANSCRIPTION UNIT

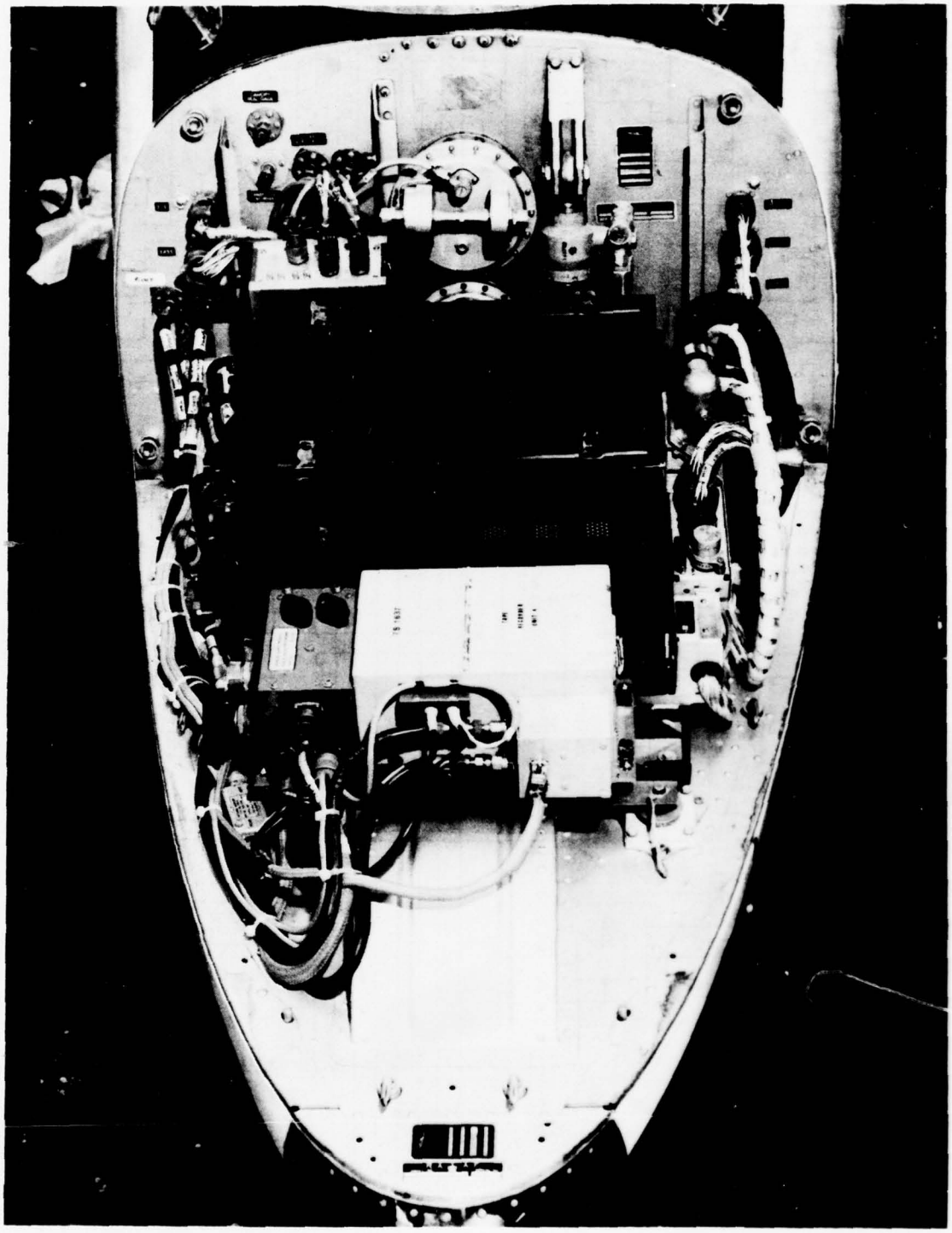


FIG. 1. DATA ACQUISITION SYSTEM COMPONENTS MOUNTED IN THE MACCHI FORWARD INSTRUMENT BAY

FIG. 2. DIGITAL DATA ACQUISITION SYSTEM FOR ENGINE CONDITION MONITORING FUNCTIONAL BLOCK DIAGRAM

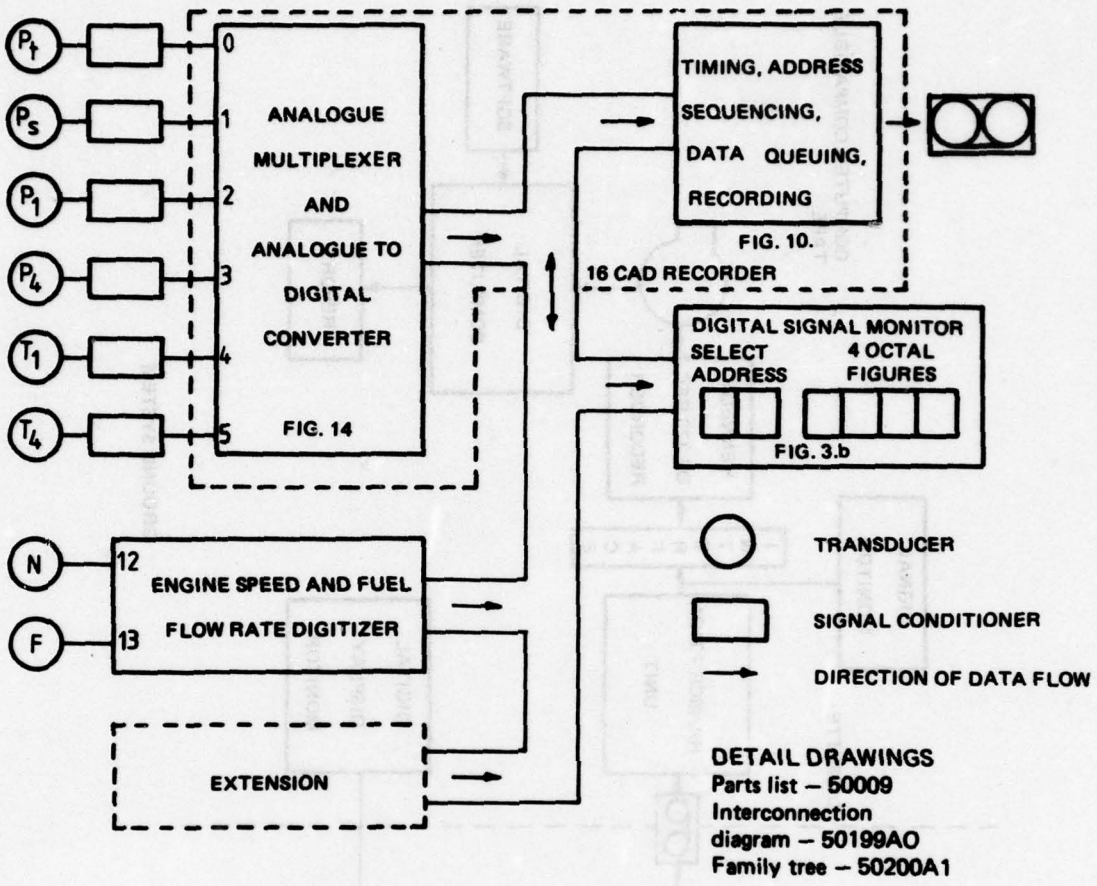


FIG. 3.a 16 CAD RECORDER AND AIRBORNE SUB-SYSTEM BLOCK SCHEMA

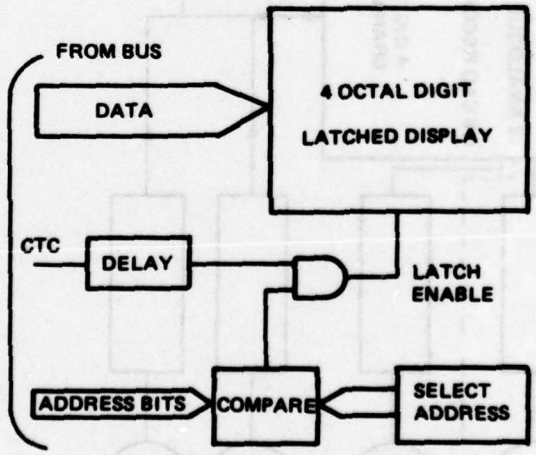


FIG. 3.b DIGITAL SIGNAL MONITOR BLOCK SCHEMA

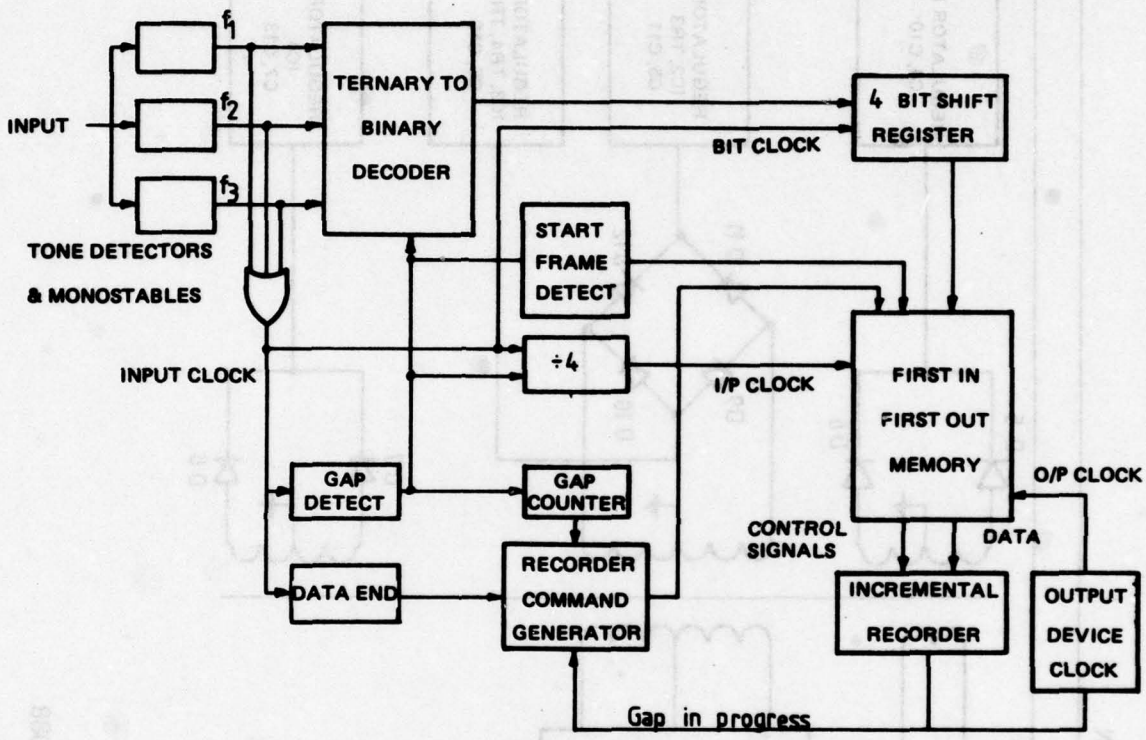


FIG. 4. TRANSCRIPTION UNIT BLOCK DIAGRAM

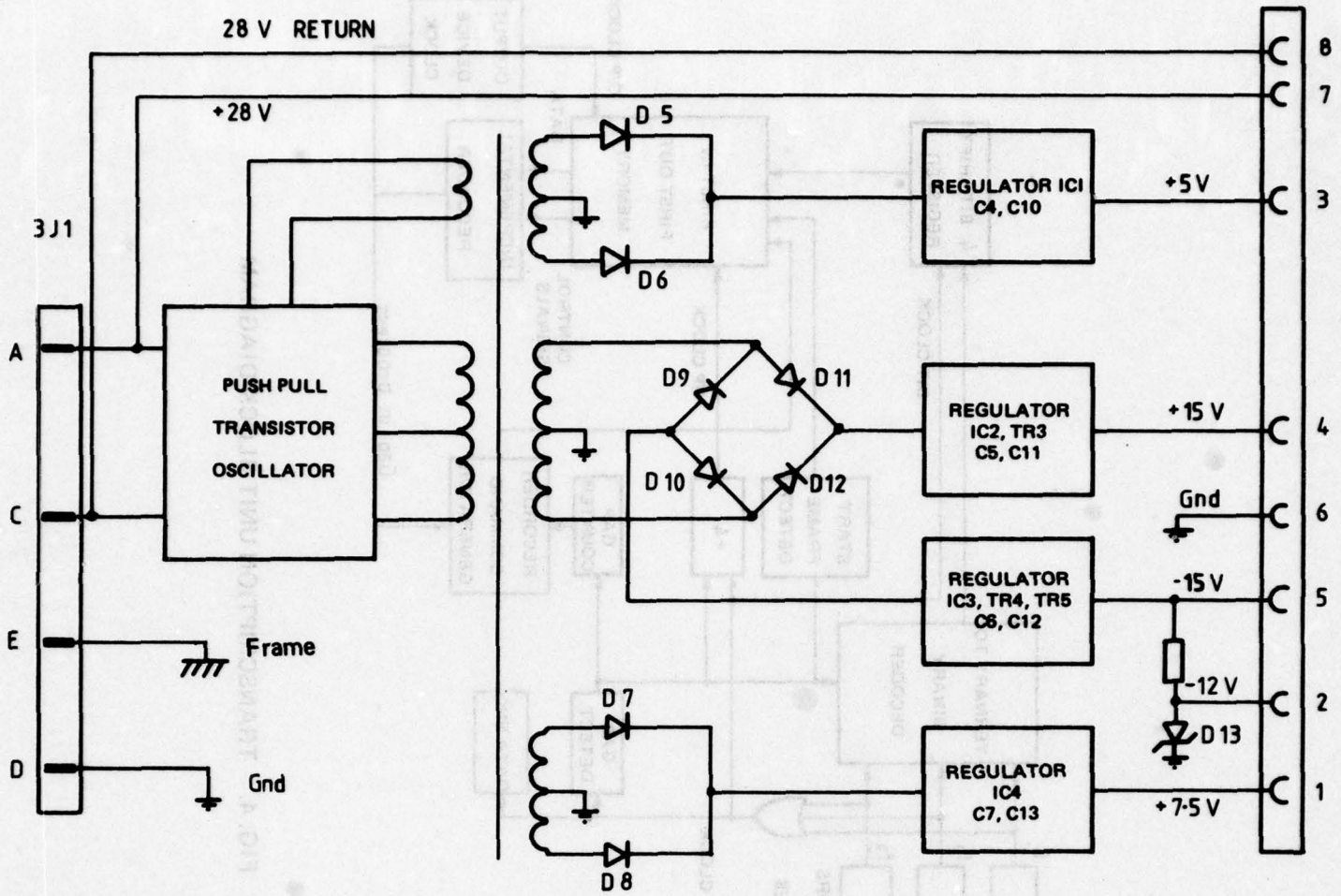


FIG. 5. 16 CAD RECORDER POWER SUPPLY SIMPLIFIED CIRCUIT

Detail drawings
Parts list – 2123
Circuit – 10453
Assembly – 10452
Interconnection – SK18088

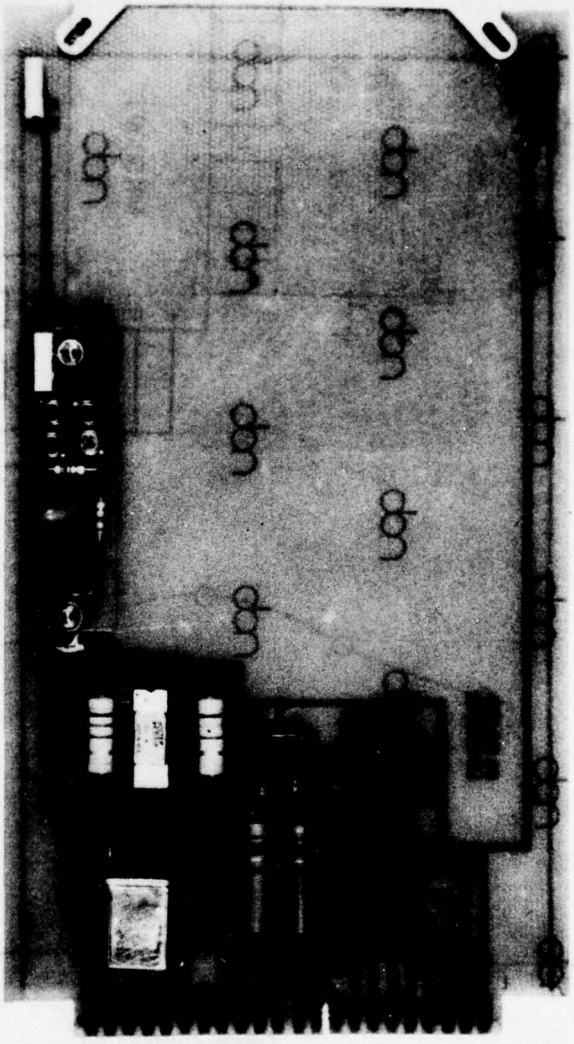


FIG. 6. CLOCK CARD

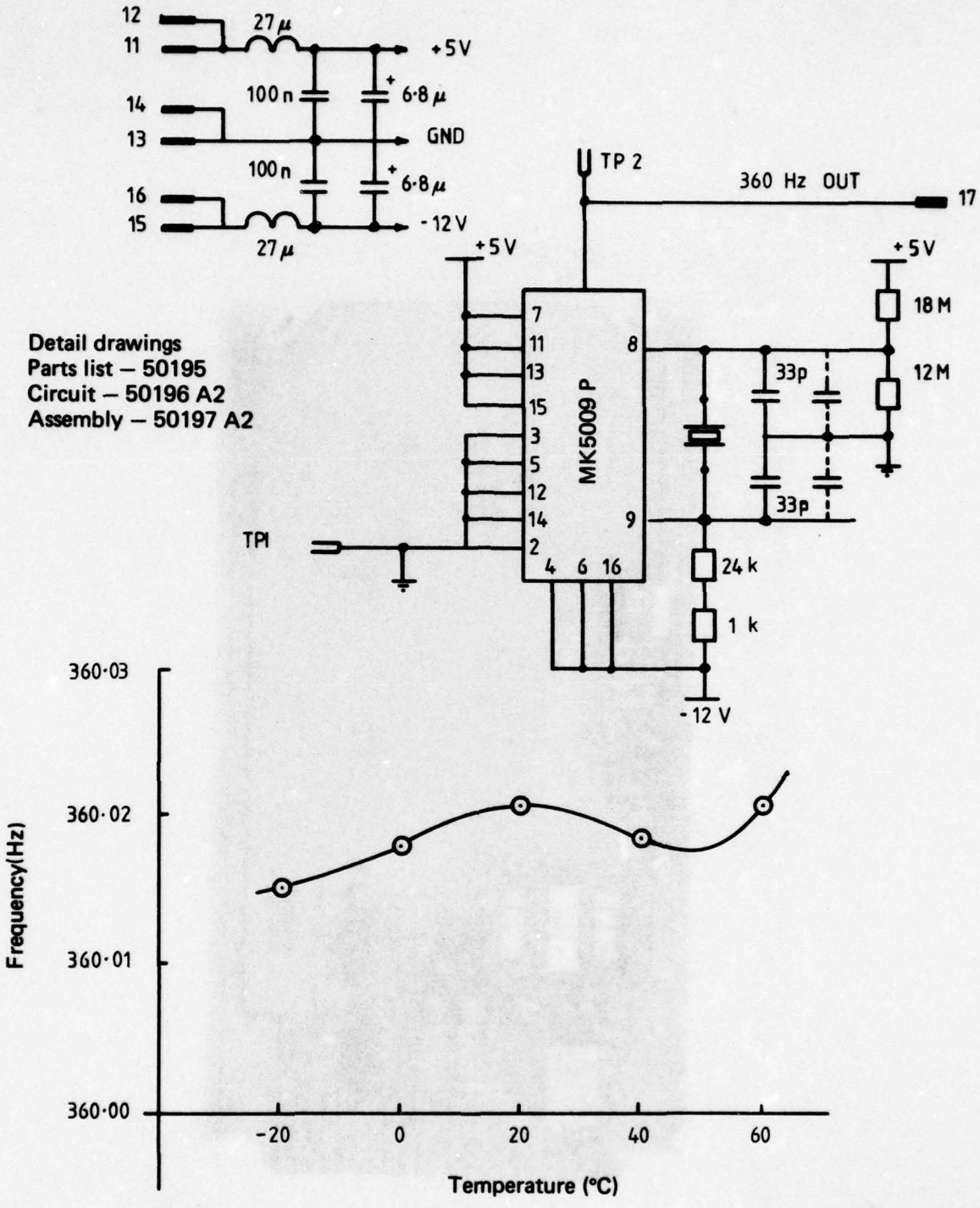


FIG. 7. 16 CAD RECORDER 360 Hz CLOCK CIRCUIT AND TEMPERATURE VARIATION

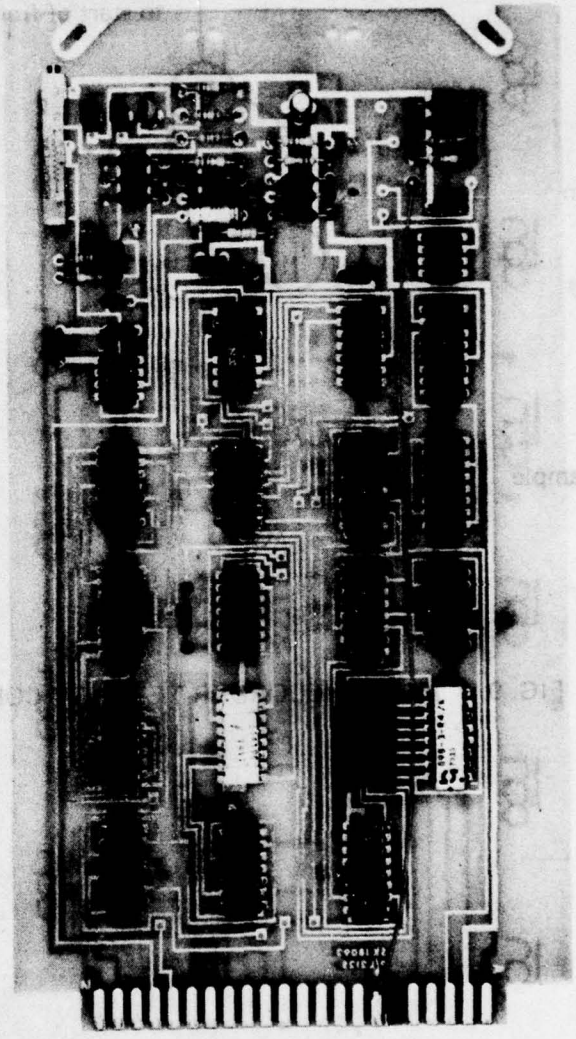
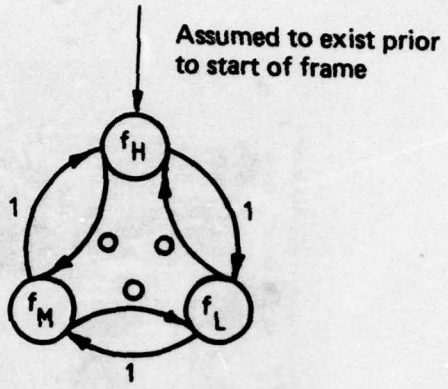


FIG. 8. DIGITAL CARD

(a) State diagram



(b) Encoding example

	1	0	0	0	1	1	1	0
(f_H)	f_L	f_H	f_M	f_L	f_M	f_H	f_L	f_H

FIG. 9. 16 CAD RECORDER TERNARY CODE

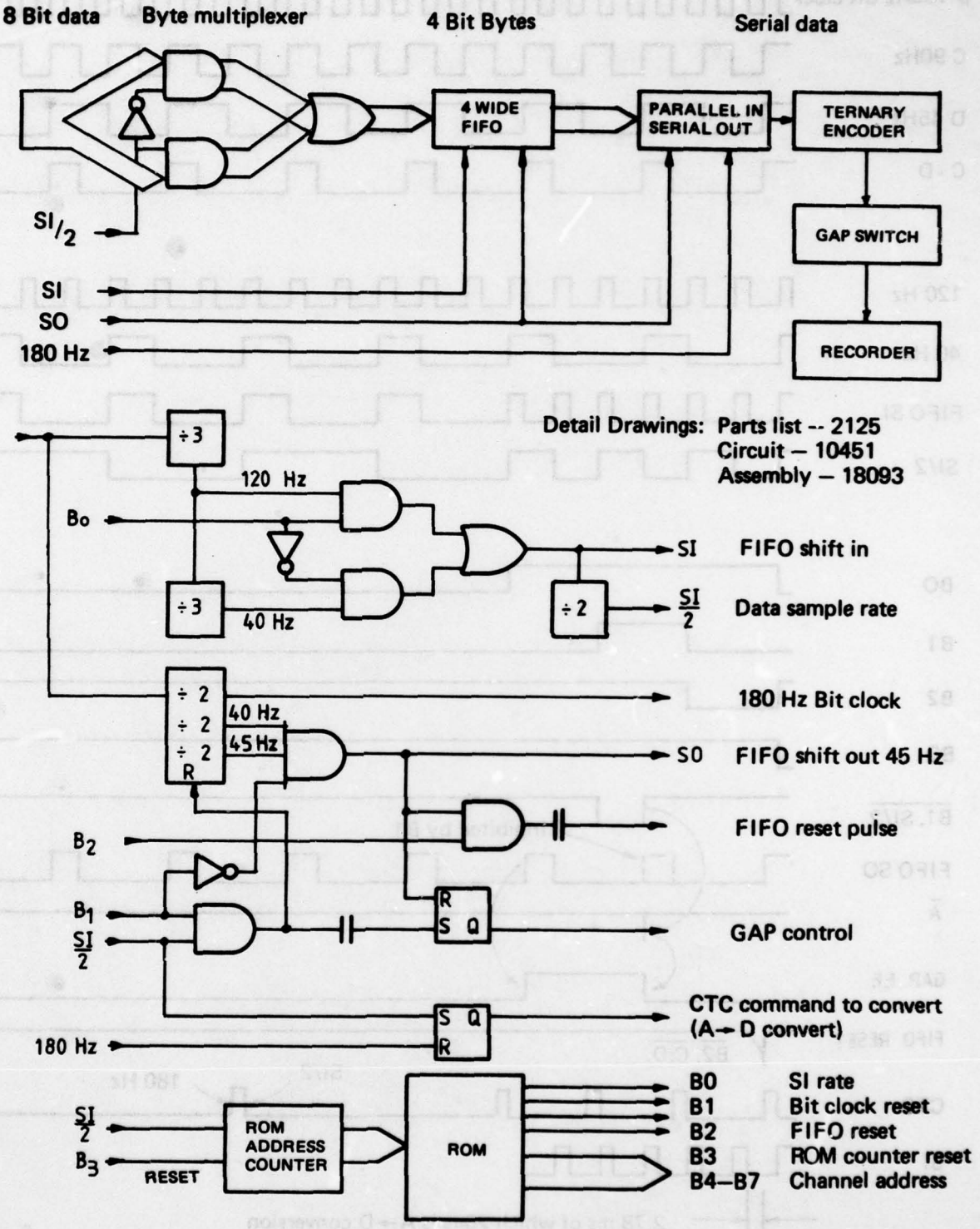


FIG. 10. 16 CAD RECORDER RECORDING CARD SIMPLIFIED SCHEMA

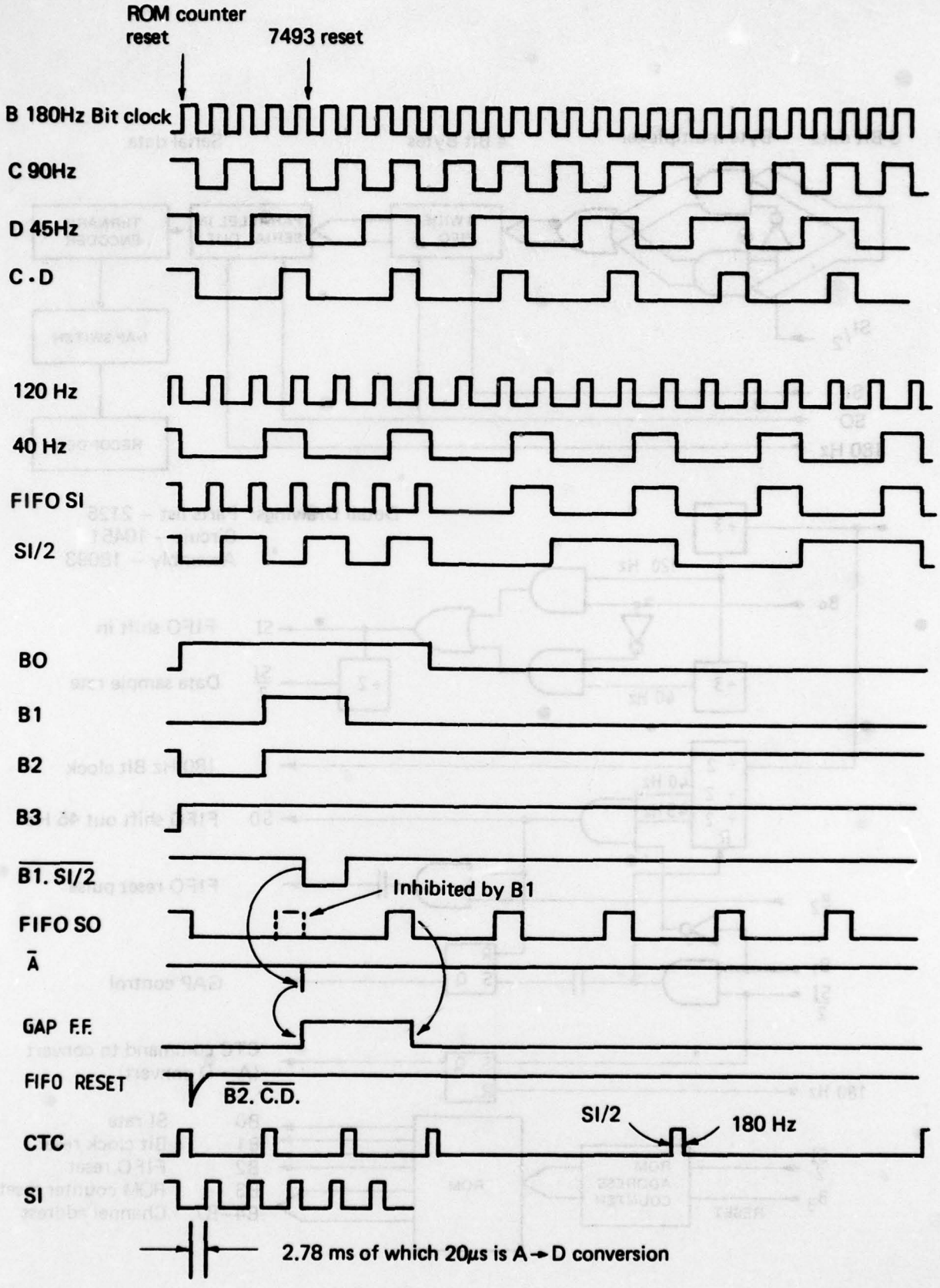


FIG. 11. RECORDING CARD WAVE FORMS

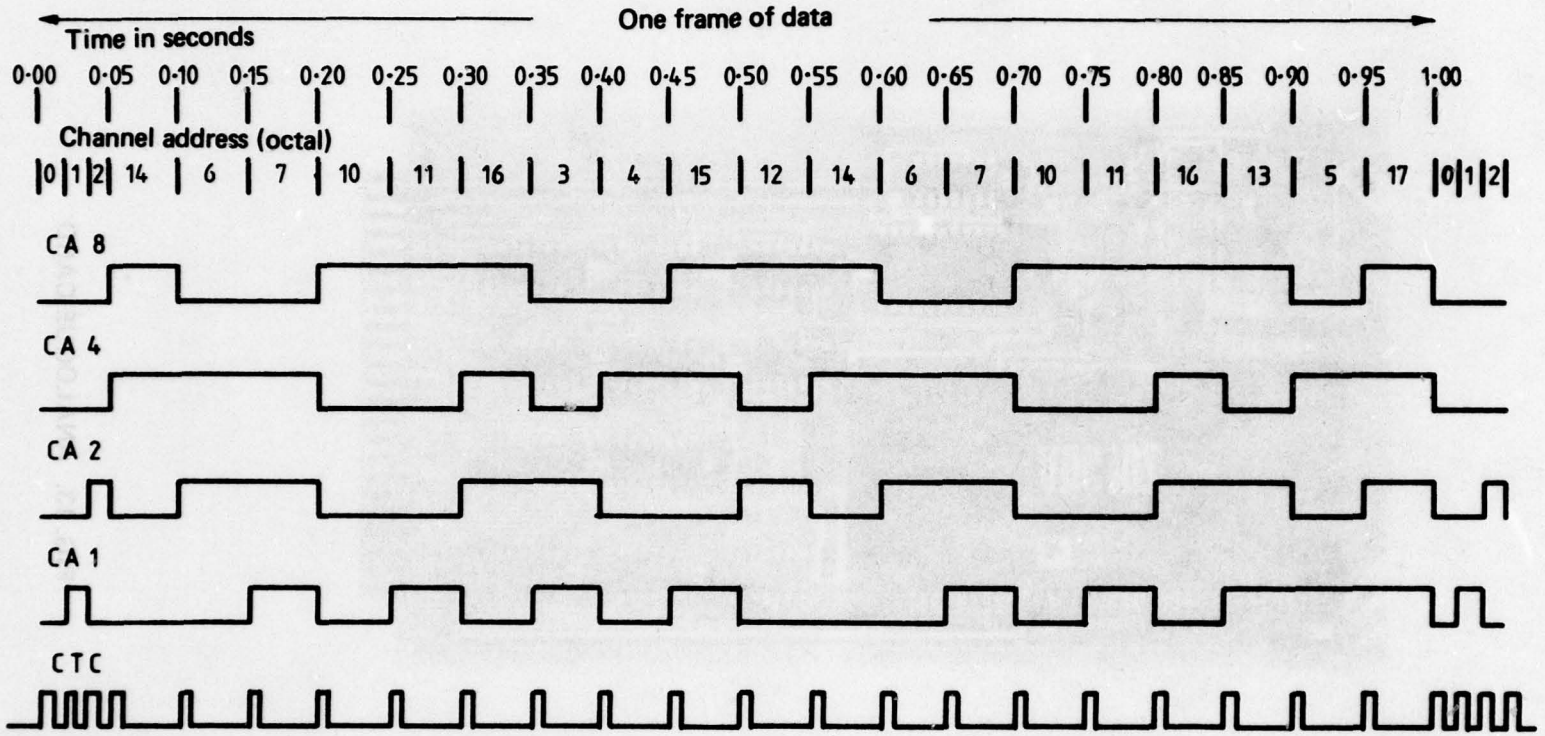


FIG. 12. INTERROGATING WAVE FORMS

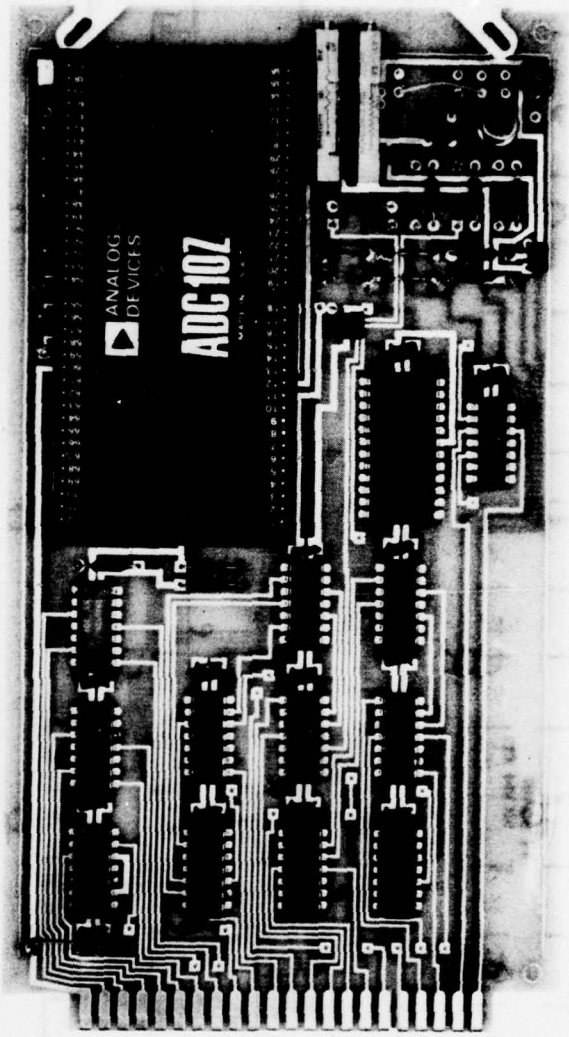


FIG. 13. ANALOGUE CARD

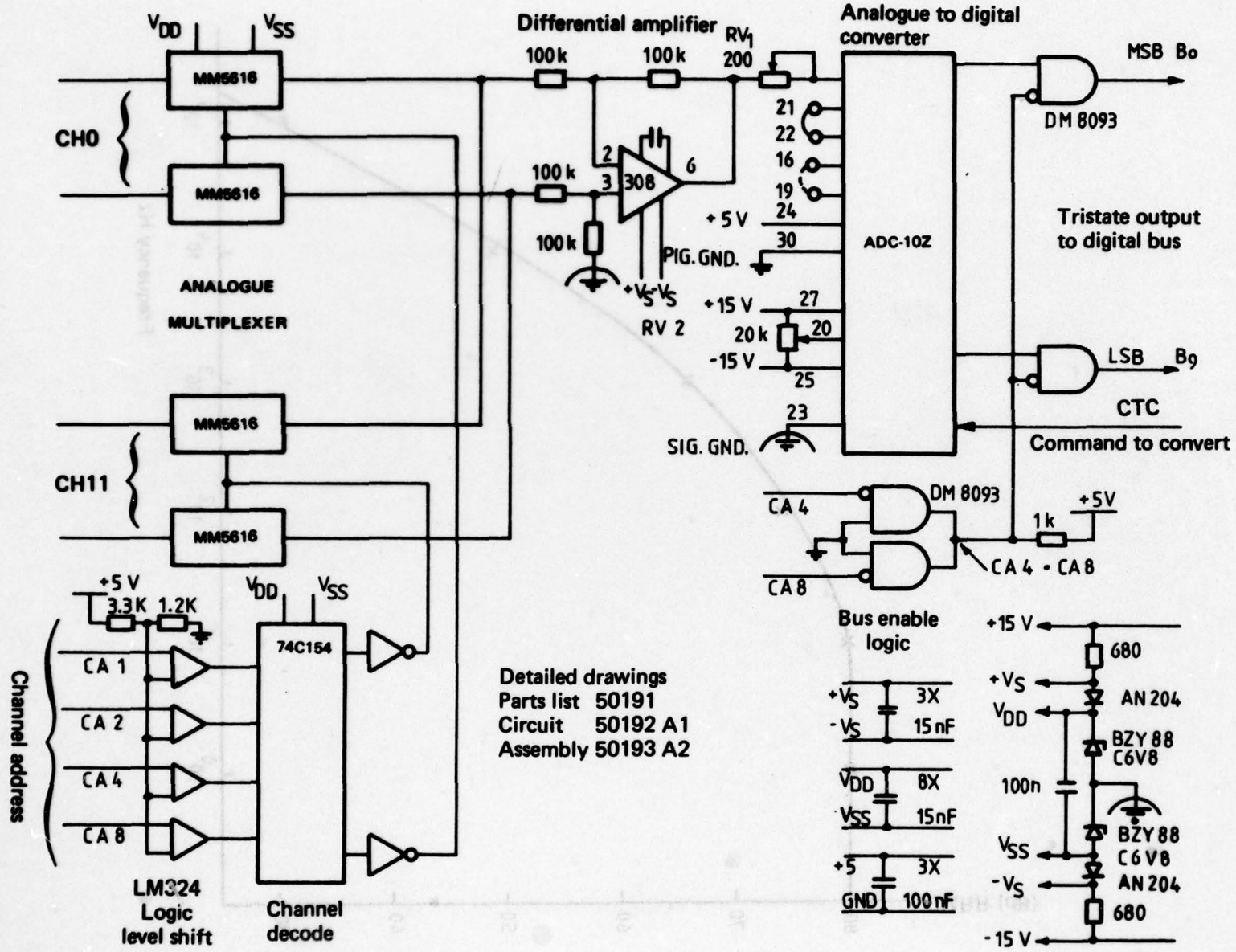


FIG. 14. ANALOGUE CARD SCHEMA

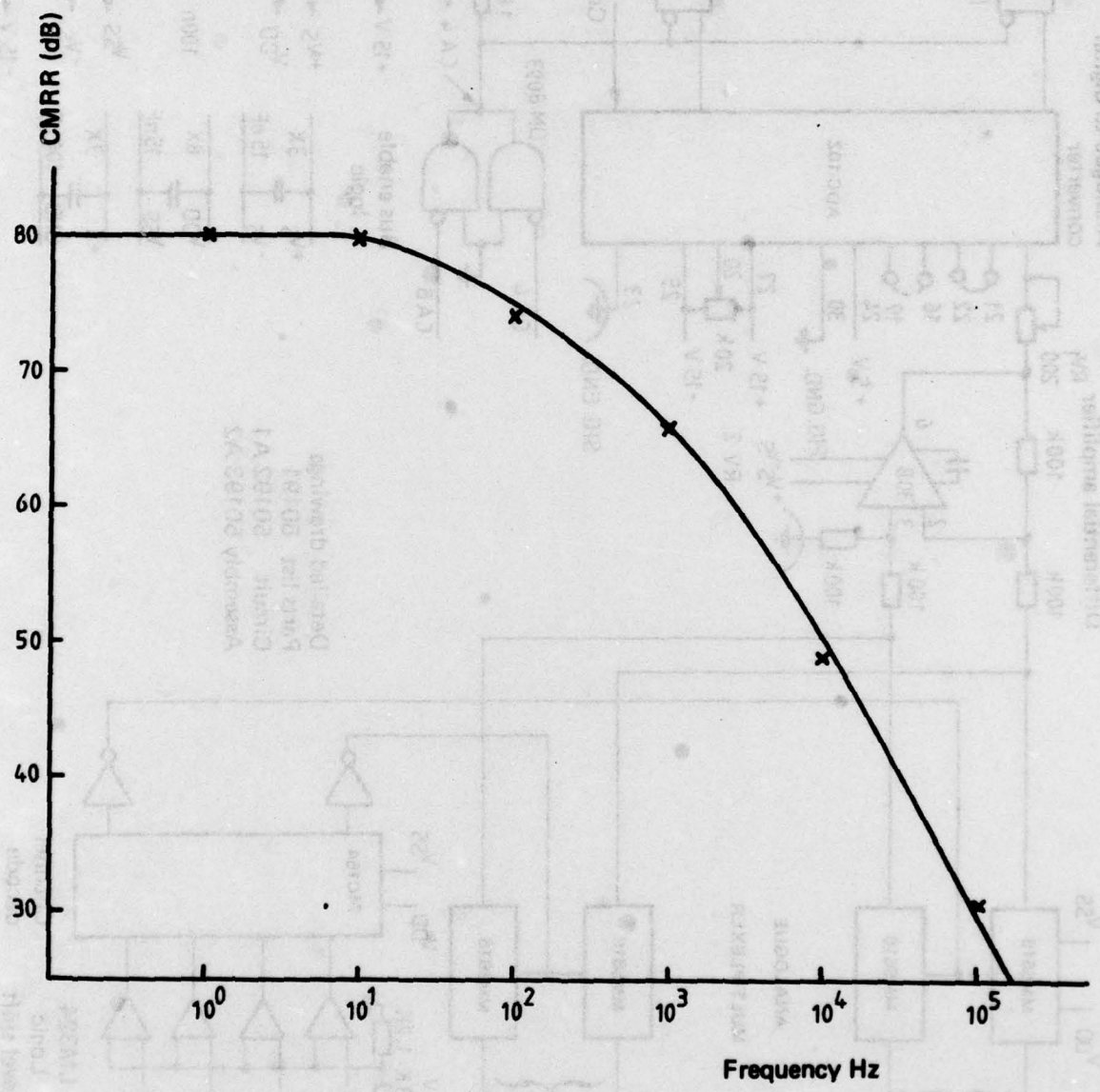


FIG. 15. ANALOGUE CARD: COMMON MODE REJECTION Versus FREQUENCY

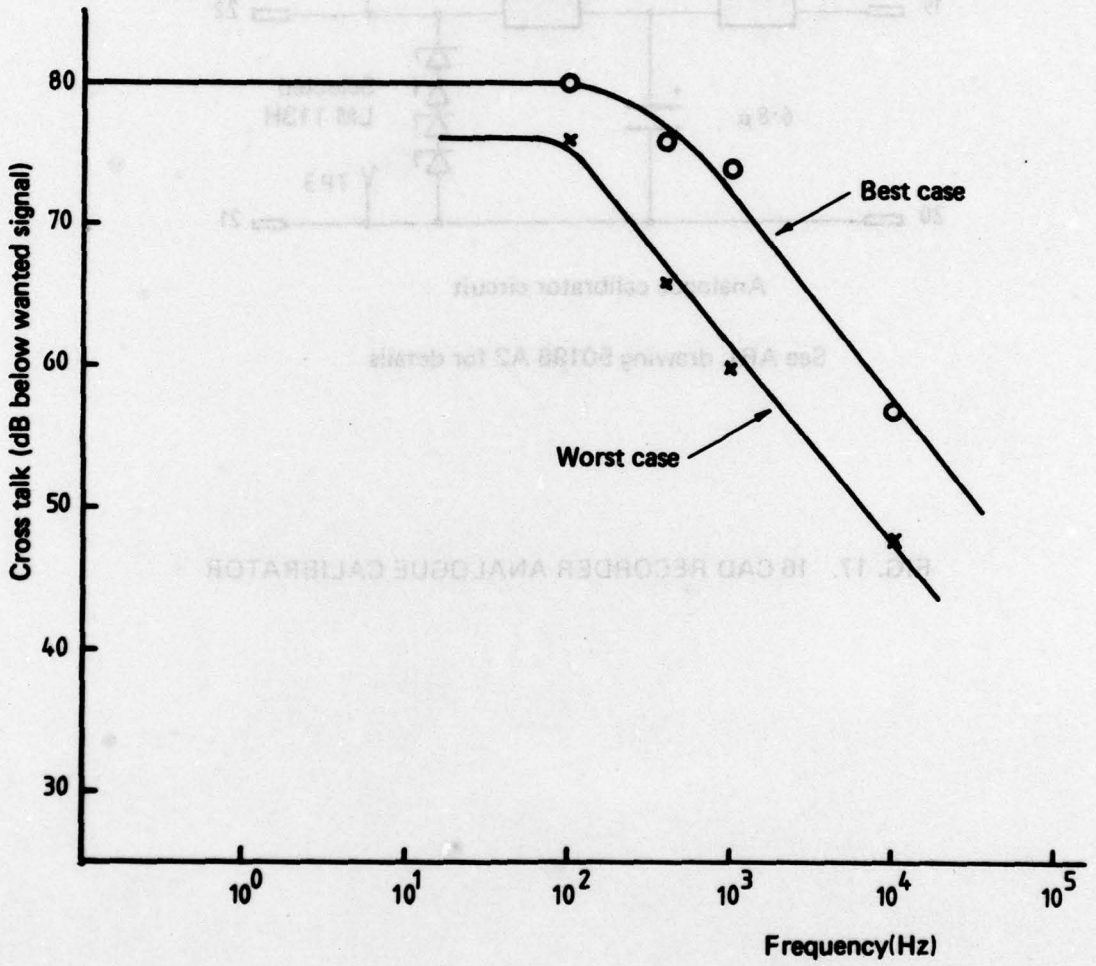
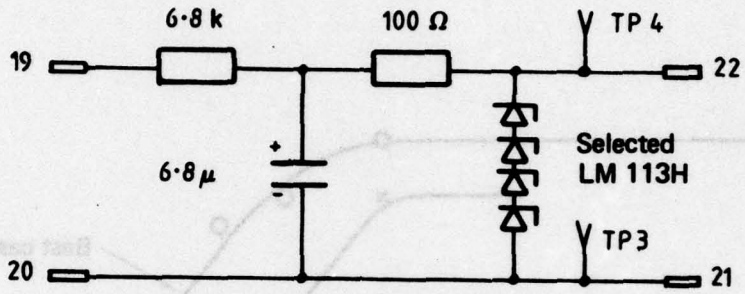


FIG. 16. ANALOGUE CARD: CROSSTALK Versus FREQUENCY



Analogue calibrator circuit

See ARL drawing 50196 A2 for details

FIG. 17. 16 CAD RECORDER ANALOGUE CALIBRATOR

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16.

ABSTRACT

A digital data acquisition system is described which has been developed as part of a project to investigate assessment of aircraft engine condition from in-flight recording of a number of parameters. The recording system is based on a small inexpensive audio tape recorder, and accepts up to 12 analogue inputs and 4 digital inputs. Recording of data in digital form is made on a standard cassette using a novel frequency coding technique. Other novel aspects of the system are the successful application of a computer-like architecture to an essentially simple system and the ease with data can be displayed for calibration and pre-flight checks with simple hand held test gear.

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